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MS-7707 Ver: 1.1 uATX(244mm X 203mm)

CPU:

INTEL -Sandy Bridge LGA 1155 (SOCKET H2)

System Chipset:

INTEL-P67 (COUGAR POINT)

OnBoard Chipset:

HD Audio Codec:ALC887-VD-GR

LAN:RTL8111E 10/100/1000

IO: Fintek F71808A

Flash ROM: 32 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel) max:8GB

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PWM:

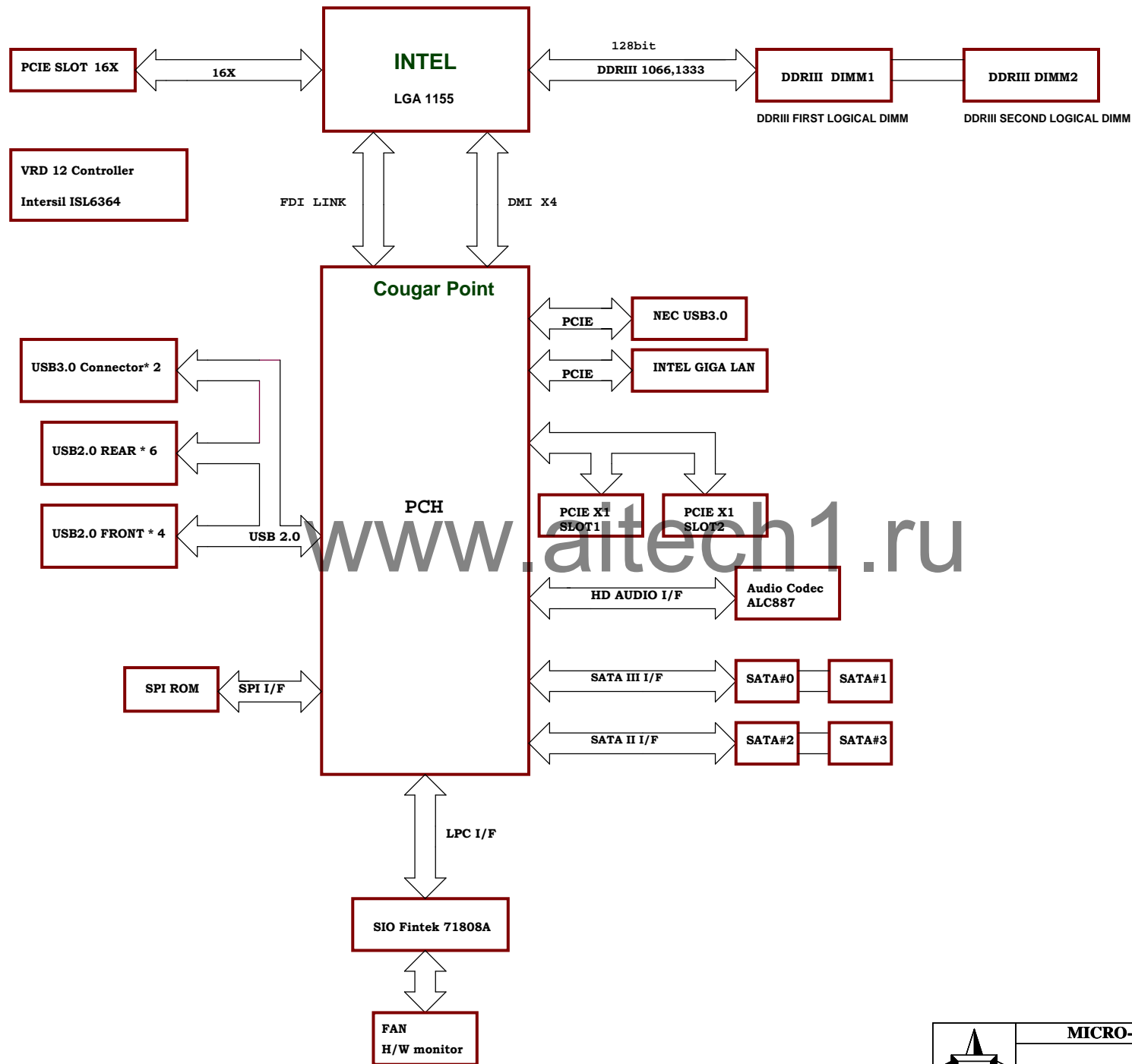
Controller:Intersil ISL6364 4-Phase -- 95W default 3 phase

Other:

SATA(SATA2-300MB/s) *2+(SATA3-600MB/s) *2

USB2.0 *12 (Rear*6 / Front*4)

USB3.0 *4 (Rear*2 / Front*2) rear or front select one



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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

TABLE 9↓
USB PORT-MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #x	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

				18BXPSAK GPIO DEFINITION	
GPIO	POWER	IO	Function	Implementation	Mother board Function
GPIO0	MAIN	1	BMBUSY#	10 K Pull-up to +3.3V	ADPT_ID_DET#
GPIO1	MAIN	1	TACH1	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH1
GPIO2	MAIN	1	PCLIRQB#	See PCA Spec	PCI Interrupt E#
GPIO3	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt F#
GPIO4	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt G#
GPIO5	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt H#
GPIO6	MAIN	1	TACH2	Pull-up to +3.3V and connect to P52 pin 12. The COMMM 8 assembly connects pin 12 directly to GND	COMM_8_DET#/ MOM_TH_ALRT#
GPIO7	MAIN	1	TACH3	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH3(PSU Fan Control)
GPIO8	RESUMB	0	ICG_B#		Reserved
GPIO9	RESUMB	1	OC5	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO10	RESUMB	1	OC6	10K Pull-up to +3.3V and connect to P126-pin 16	PRNTR_DET#
GPIO11	RESUMB	1	SMBALERT#	20K Pull-up to +3.3VSB. It is always enabled as a wake event.	SMBALERT#
GPIO12	RESUMB	1	LAN_DISABLE	Follow implementation in Intel Picton Design Guide	LAN_DISABLE#
GPIO13	RESUMB	1	IO_PMB	10K Pull-up to +3.3V and connect to P151-pin 10; also add a no-installed pull-down to the net.	RDYBST_DET# or DASH SMI
GPIO14	RESUMB	1	OC7	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation. 8.2K Pull-up to +3.3V and connect to the SMI pin on the SIO	SMI# from SIO
GPIO15	RESUMB	1	PCB_GPIO15		Reserved
GPIO16	RESUMB	0	SATA2DP	10 M pull-up to VBAT and connect to CPU SKT0CC#, SIO pin48 and PCH	CPU_MISSING
GPIO17	MAIN	1	TACH0	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH0(Front Chassis Fan)
GPIO18	MAIN	1	PCIECLKQ#	Through a 1KΩ series resistor, 8.2K pull-up to +3.3V and connect to E15-pin 1. E15 Pin 2 connect to GND	BOOT_BLK_REC#
GPIO19	MAIN	1	SATA1DP	connect to a test point	unused
GPIO20	MAIN	1	PCIECLKQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to HANKSVILLE -pin48	PCIECLKQ2#
GPIO21	MAIN	1	SATA2DP	10K pull-up to +3.3V and connect to P23-pin 4.	FRNT_AUD_DET#
GPIO22	MAIN	1	SCLOCK	10K Pull-up to +3.3V and connect to P160-pin 10	INT_USB_DET#
GPIO23	MAIN	1	LDQ#	connect to a test point.	PEG_MOM_DET#
GPIO24	RESUMB	0	MBALED	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to P125-Pin 1. 1M pull-up to VBAT and connect to P125-pin 3	HOOD_SW_DET#
GPIO25	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKQ3#
GPIO26	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKQ4#
GPIO27	RESUMB	0	OD_PLL_VR_EN	10K pull-up to +3.3VAUX	Reserved
GPIO28	RESUMB	0	PCB_GP28	connect to a test point	unused
GPIO29	RESUMB	0	SLP_LAN#	refer to the PCA spec.	SLP_LAN#
GPIO30	RESUMB	1	SUS_PWRACK	100K Pull-up to 3.3V_AUX	unused
GPIO31	MAIN	1	ACPRESENT	10K Pull-up to +3.3V and connect to P25-pin 10	FRONT_USB_DET1#
GPIO32	MAIN	0	PCB_GP32	Through a 1kΩ series resistor, 10K pull-up to +3.3V and connect to P2-pin 6.	NON-EPA_PS_DET#

GPIO33	MAIN	0	PCB_GP33	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to pin 1 of jumper E1 and E1 pin2 to GND	FDT_OVRD#
GPIO34	MAIN	0	SP_PC#	3.3K Pull-down to GND and connect to P124-pin 2. Decouple P124-pin 2 with 0.1μF P124 pin 1 2.2K pull-up to 5V and P124 pin 6 2.2k pull-up to 5V	HOOD_LOCK_DET
GPIO35	MAIN	0	SATACLKREQ#	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV0
GPIO36	MAIN	1	SATA2DP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1
GPIO37	MAIN	1	SATA3DP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2
GPIO38	MAIN	1	SLOAD	Through a series 1K resistor, 10K Pull-up to +3.3V and 10K pull-down to GND and connect to P5-pin 9. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID0
GPIO39	MAIN	1	SDATAOUT0	Pull-up to +3.3V and connect to top-layer ring of PCA mounting hole used for SFF Basepan detect feature.	BRD_ID1
GPIO40	RESUMB	1	OC1	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for XDP implementation. 8.2kΩ pull-down to GND and connect to E49-pin 2 E49 pin-1 300 pull-up to +3.3V	PASSWORD_EN
GPIO41	RESUMB	1	OC2	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO42	RESUMB	1	OC3	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO43	RESUMB	1	OC4	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO44	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3VAUX and connect to a test point.	PCIECLKQ6#
GPIO45	RESUMB	1	PCIECLKQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to J3-pin8 J7	PRSN#_J31
GPIO46	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKQ7#
GPIO47	RESUMB	1	PBG_A_CLKQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to J4-pin848 and B81	PRSN#_J41
GPIO48	MAIN	1	SDATAOUT1	Through a series 1K resistor, 10K Pull-up to +3.3V and 10K pull-down to GND and connect to P5-pin 10. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID1
GPIO49	MAIN	0	SATA3DP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0
GPIO50	MAIN	1	PCLIRQ#1	8.2k pull-up to VCC3	REQ1#
GPIO51	MAIN	0	PCLQNT#1	connect to a test point	GNT1#
GPIO52	MAIN	1	PCLIRQ#2	8.2k pull-up to VCC3	REQ2#
GPIO53	MAIN	0	PCLQNT#2	connect to a test point	GNT2#
GPIO54	MAIN	1	PCLIRQ#3	Through a 8.2KΩ series resistor, connect to E14-pin 2 and 1K pull-down to GND. E14-pin1 connect to +3.3V	BOOT_BLK_EN#
GPIO55	MAIN	0	PCLQNT#3	connect to a test point	GNT3#
GPIO56	RESUMB	1	PBG_B_CLKQ#	refer to the PCA spec.	AUD_AMP_DIS#
GPIO57	MAIN	1	PCB_GP57	10K Pull-up to +3.3VME installed and 10K pull-down to GND not installed.	TPM_PP

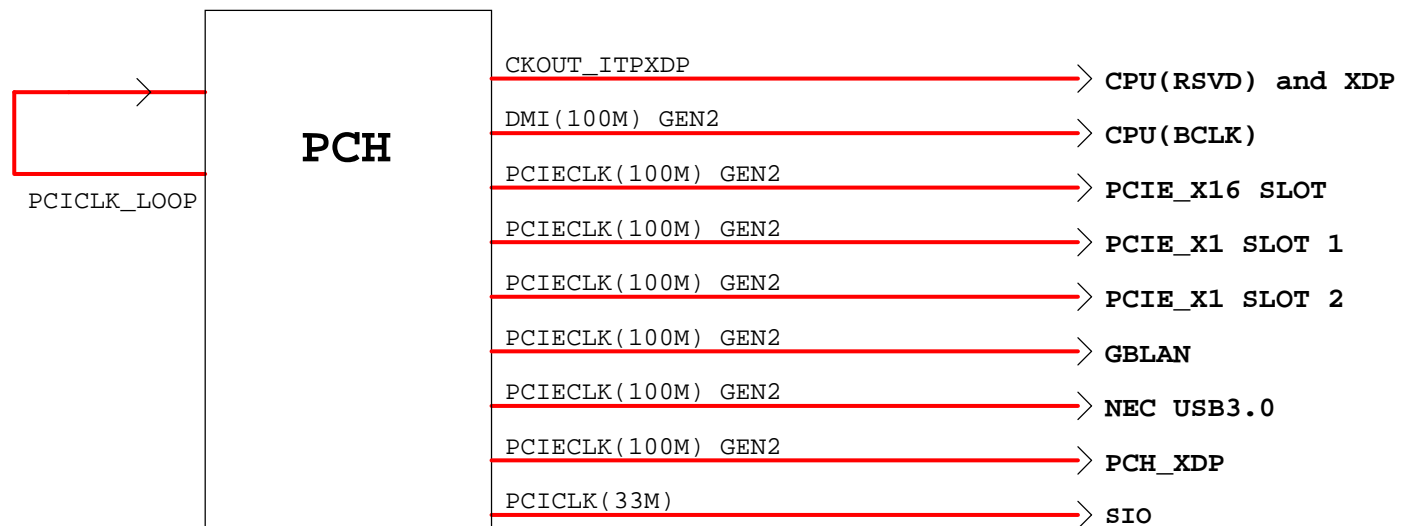
GPIO58	RESUMB	0	SMCLK	10K pull-up to 3V_AUX	SMCLK
GPIO59	RESUMB	1	OC0	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO60	RESUMB	0	SMDALBRT#	10K pull-up to 3V_AUX	SMDALARM
GPIO61	RESUMB	0	SUS_STAT#	connect to a test pin	LPCPD#
GPIO62	RESUMB	0	SUSCLK	SUSCLK to SIO-pin16	SUSCLK
GPIO63	RESUMB	0	SLP_S#	Connect to the SIO-pin37	SLP_S#
GPIO64	MAIN	0	CLKOUTFLBK0	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK0
GPIO65	MAIN	0	CLKOUTFLBK1	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK1
GPIO66	MAIN	0	CLKOUTFLBK2	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK2
GPIO67	MAIN	0	CLKOUTFLBK3	refer to the PCA spec. unused clock connect to a test point	CLK14M
GPIO72	RESUMB	1	PCB_GP72	Pull-up to +3.3V and connect to P24-pin 10	FRONT_USB_DET0#
GPIO73	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3VAUX and through a 0Ω series resistor, connect to J42-pin8 J7, B31, B48, and B81	PRSN#_J42
GPIO74	RESUMB	0	SMDALBRT#	10K pull-up to 3V_AUX	SMDALERT#
GPIO75	RESUMB	0	SMDLIDATA	10K pull-up to 3V_AUX	SMDLIDATA



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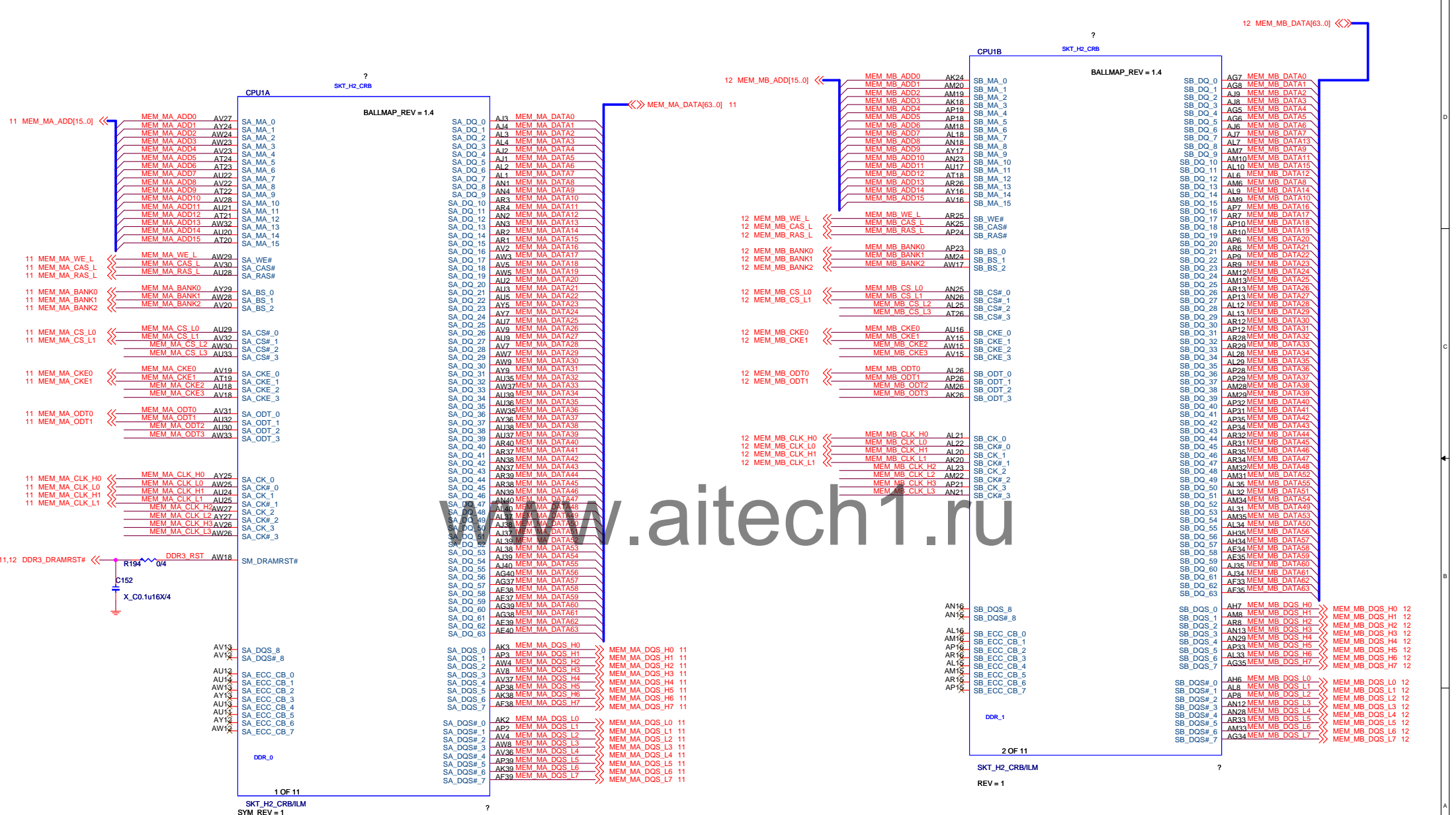
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X'TAL
25 MHz

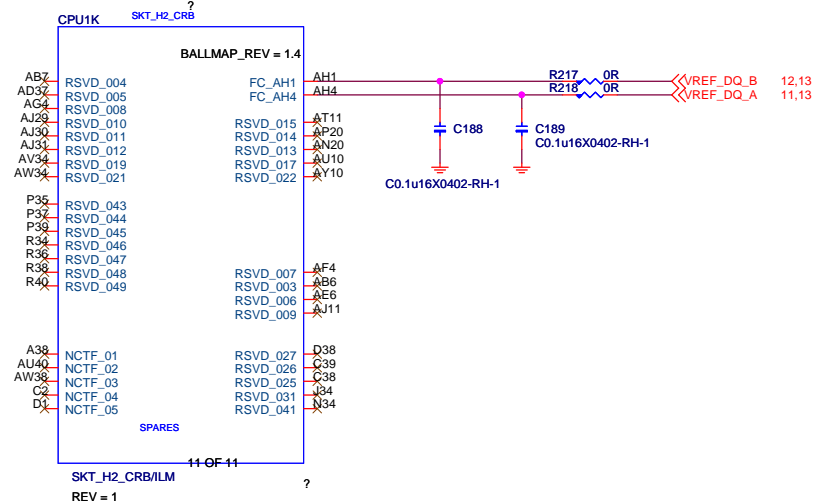
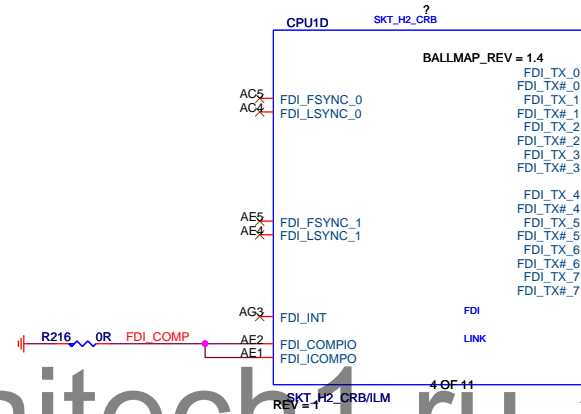
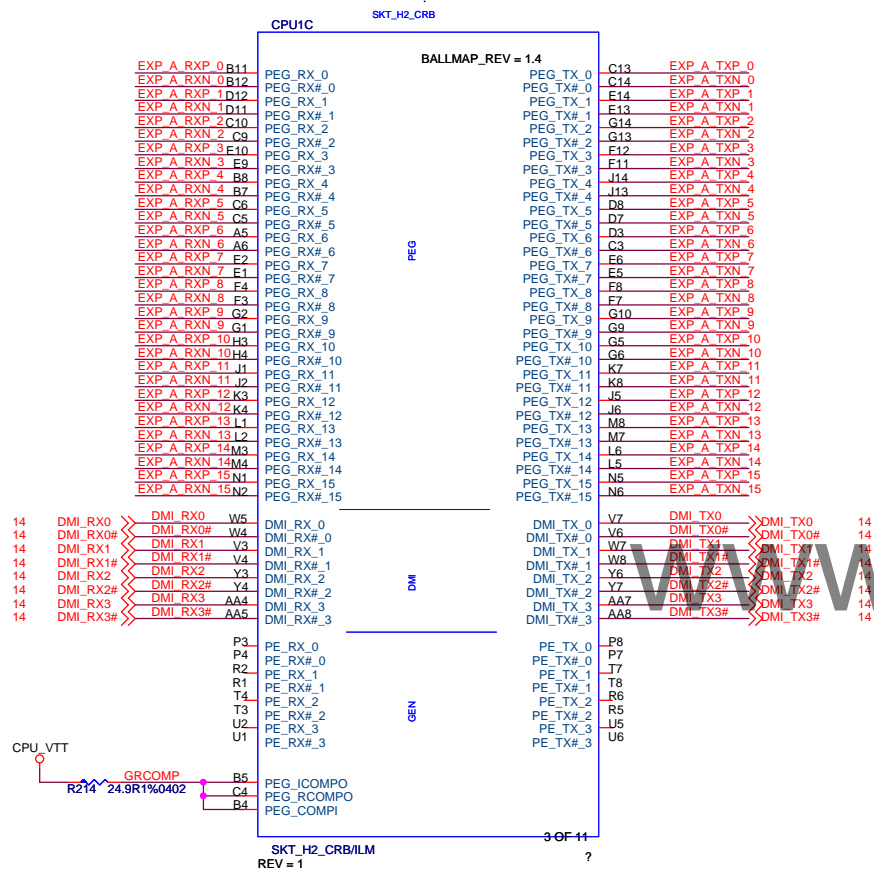
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6.1.4.2 FDI Disable Guidelines

All the FDI signals FDI_TX, FDI_FSYNC, FDI_LSYNC and FDI_INT signals on the CPU and the PCH can be left as No connect for solutions not using integrated graphics solution.

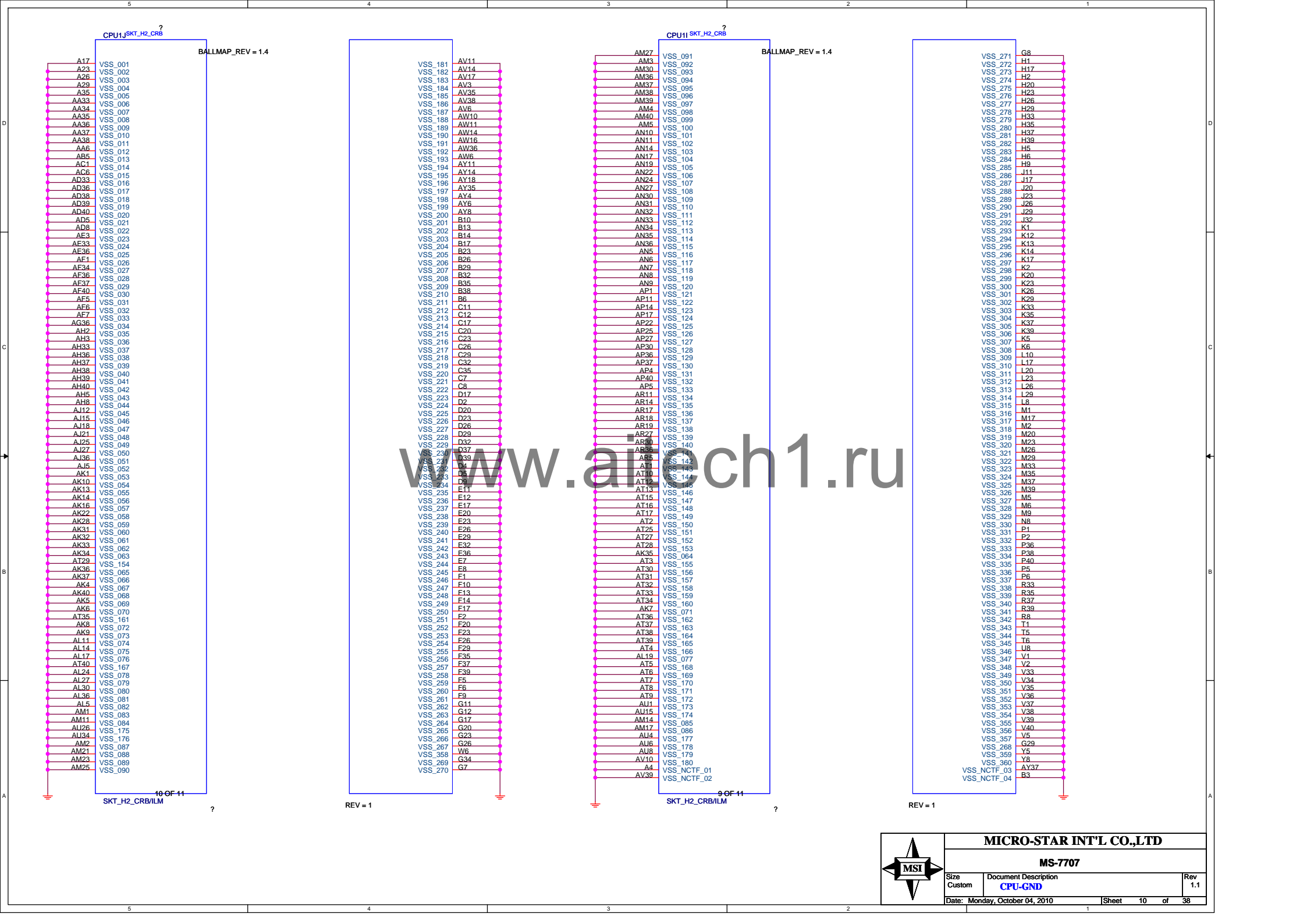
FDI Signal	Recommendation
FDI_TX[7:0]	Float or No connect
FDI_TX#[7:0]	Float or No connect
FDI_FSYNC [1:0]	Float or No connect
FDI_LSYNC [1:0]	Float or No connect
FDI_INT	Float or No connect
FDI_COMPIO	Connect to Vss
FDI_ICOMPO	Connect to Vss



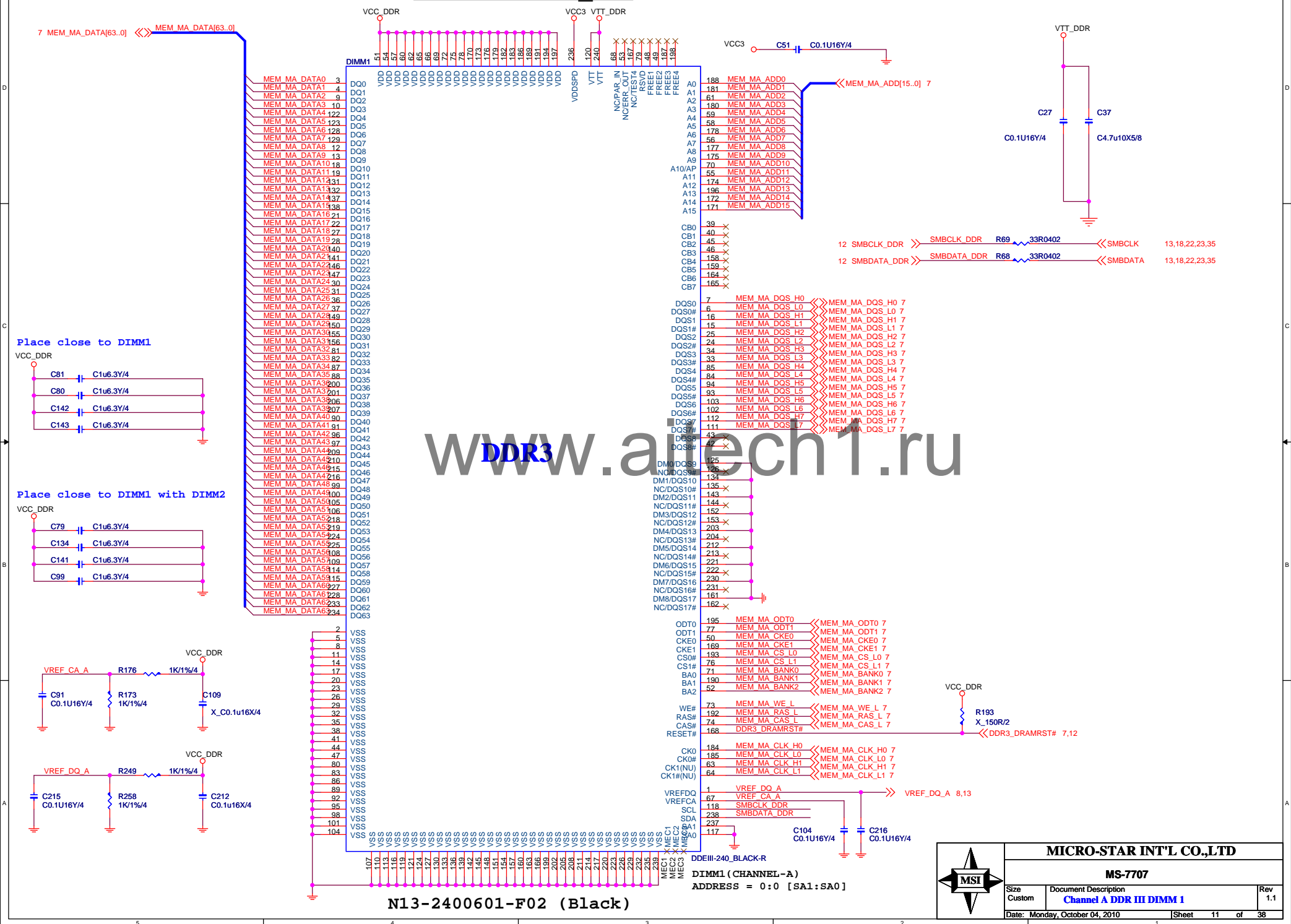
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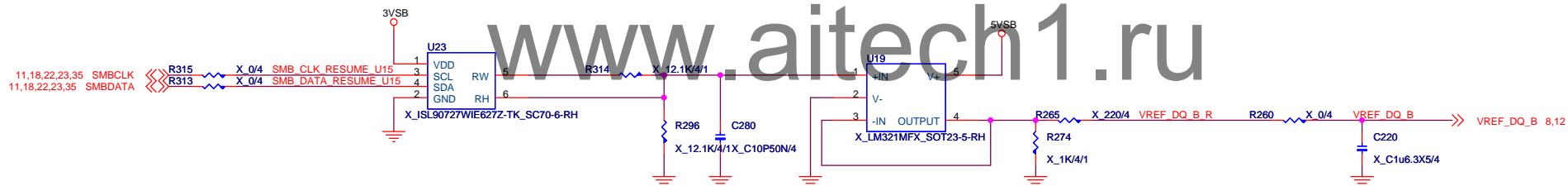
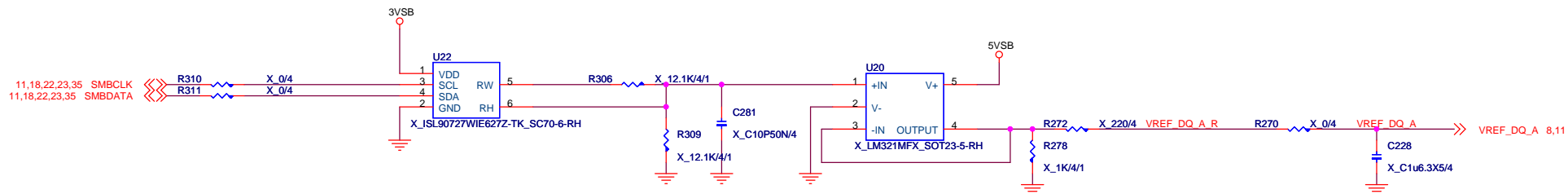
DDRIII DIMM A1



DDR3



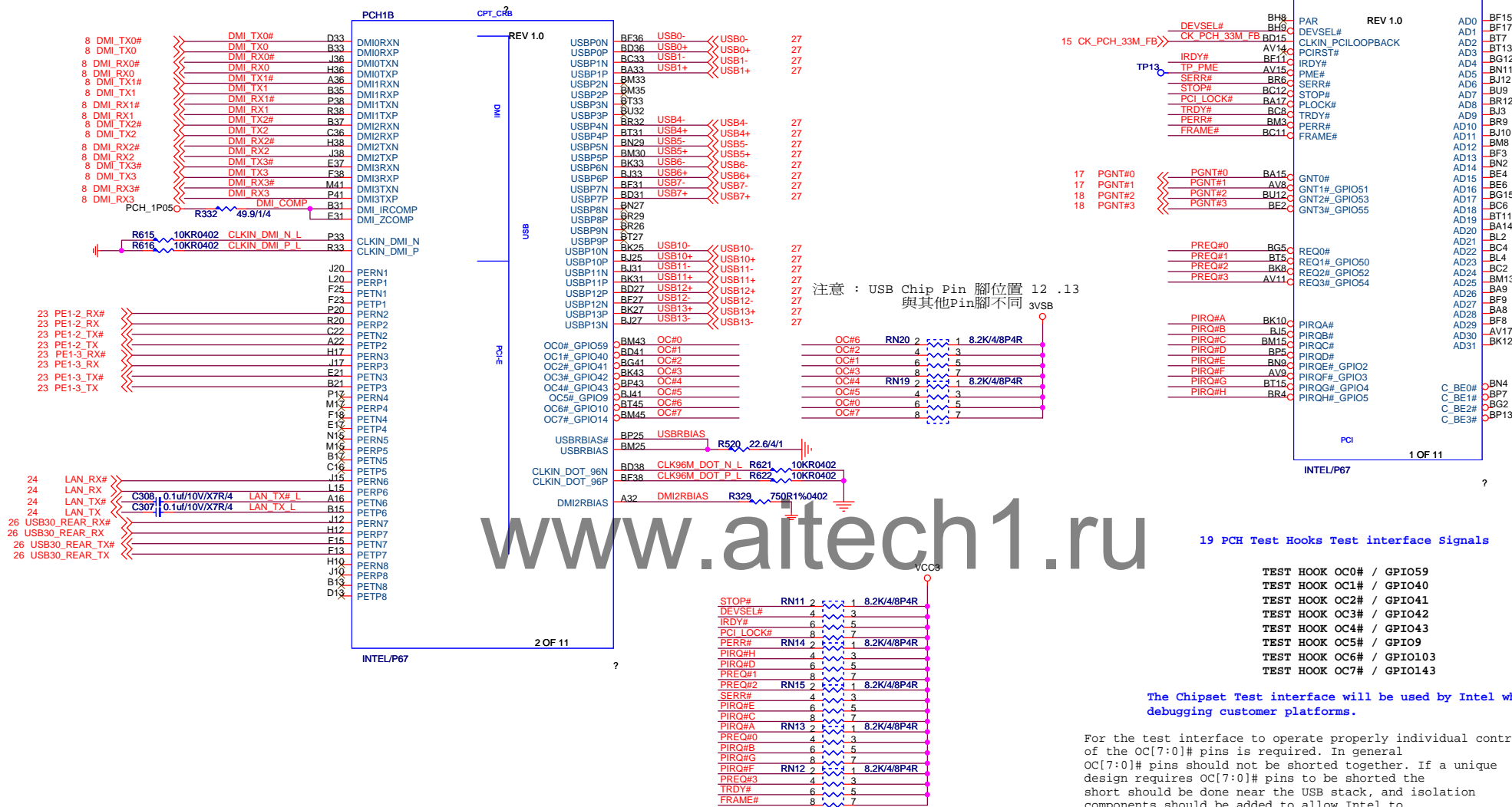
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PCH H67 料號



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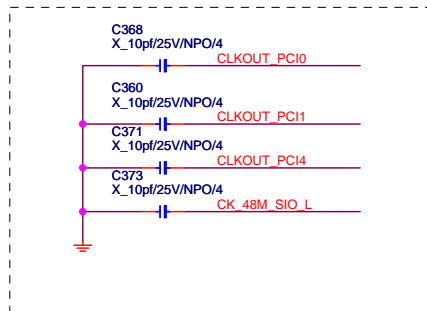
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21 CK_P_33M_SIO_PCH << R415 22R/4 CLKOUT_PCI0 AT11 CLKOUT_PCI0
 21 CK_P_33M_SIO_DEBUG << R409 22R/4 CLKOUT_PCI1 AN14 CLKOUT_PCI1
 TP8 CLKOUT_PCI2 AT12 CLKOUT_PCI2
 TP10 CLKOUT_PCI3 AT17 CLKOUT_PCI3
 14 CK_PCH_33M_FB << 22R0402 R426 CLKOUT_PCI4 AT14 CLKOUT_PCI4
PCICLK LOOPBACK

21 CK_48M_SIO << R422 33/4 CK_48M_SIO_L
 PCH_1P05 R619 90.9R1%0402 XCLK_RCOMP AL2 XCLK_RCOMP
 CLK14M_PCH AN8 REFCLK14IN
 R620 10K/4

C27p50N C343 XTAL_25M_PCH_OUT AJ5 XTAL25_OUT
 25MHZ18P_D-1 Y3 1MR0402 R386 XTAL25_IN AJ3
 C27p50N C355 XTAL_25M_PCH_IN

EMI Result



PCH1H CPT_CRB

REV 1.0

CLKIN_GND1_N R27 CK 100M_CPHY_PCH_IN_DN_L R614 10K/4
 CLKIN_GND1_P R27 CK 100M_CPHY_PCH_IN_DP_L R613 10K/4
 CLKIN_GND0_N W53 CK CSI_PCH_IN_DN_L R618 10K/4
 CLKIN_GND0_P V52 CK CSI_PCH_IN_DP_L R617 10K/4
 CLKOUT_ITP_XDP_N R52 CK ITP_CLKINN_L R338 0/4 >>>CK_ITP_CLKINN 6
 CLKOUT_ITP_XDP_P N52 CK ITP_CLKINP_L R337 0/4 >>>CK_ITP_CLKINP 6
 CLKOUT_PCIE7N AE2 X 0/4 >>>CK_XDP_DN 35
 CLKOUT_PCIE7P AF1 X 0/4 >>>CK_XDP_DP 35
 CLKOUT_DMI_N P31 CK PE_DMI_DN_L R323 0/4 >>>CK_PE_DMI_DN 6
 CLKOUT_DMI_P R31 CK PE_DMI_DP_L R324 0/4 >>>CK_PE_DMI_DP 6
 CLKOUT_DP_N N56
 CLKOUT_DP_P X55
 CLKOUT_PCIE0N AE6 CK RTL_GLAN_DN_L R385 0/4 >>>CK_RTL_GLAN_DN 24
 CLKOUT_PCIE0P AC6 CK RTL_GLAN_DP_L R380 0/4 >>>CK_RTL_GLAN_DP 24
 CLKOUT_PCIE1N AA5 CK_PEX1-2N_L R363 0/4 >>>CK_PEX1-2N 23
 CLKOUT_PCIE1P W5 CK_PEX1-2P_L R360 0/4 >>>CK_PEX1-2P 23
 CLKOUT_PCIE2N AB12 CK_PEX1-3N_L R344 0/4 >>>CK_PEX1-3N 23
 CLKOUT_PCIE2P AB14 CK_PEX1-3P_L R343 0/4 >>>CK_PEX1-3P 23
 CLKOUT_PCIE3N AB9
 CLKOUT_PCIE3P AB8
 CLKOUT_PCIE4N Y9 CK_NEG_R_USB_DN_L R387 0/4 >>>CK_NEG_R_USB_DN 26
 CLKOUT_PCIE4P Y8 CK_NEG_R_USB_PN_L R381 0/4 >>>CK_NEG_R_USB_PN 26
 CLKOUT_PCIE5N AF3
 CLKOUT_PCIE5P AG2
 CLKOUT_PCIE6N AB3 CK_PCH_XDP_N TP16
 CLKOUT_PCIE6P AA2 CK_PCH_XDP_P TP17
 CLKOUT_PEG_A_N AG8 CK_16PORT_DN_L R350 0/4 >>>CK_16PORT_DN 22
 CLKOUT_PEG_A_P AG9 CK_16PORT_DP_L R346 0/4 >>>CK_16PORT_DP 22
 CLKOUT_PEG_B_N AE12
 CLKOUT_PEG_B_P AE11

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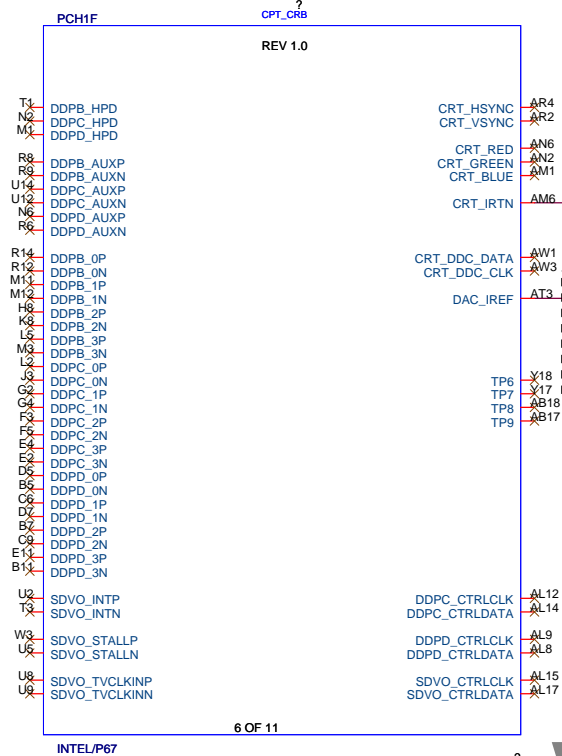
INTEL/P67



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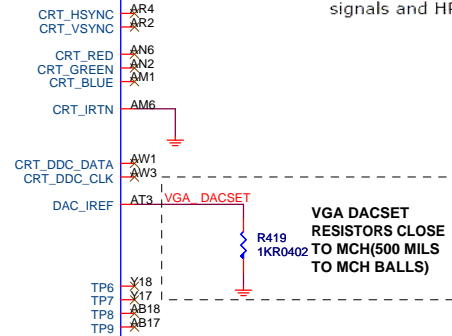
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7.1.7 DisplayPort Disable

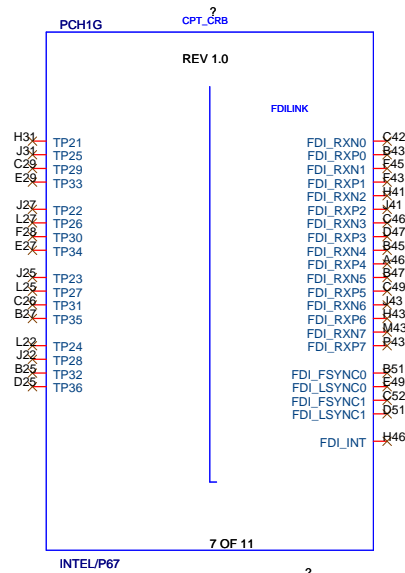
If DisplayPort interface is not implemented, the Main Link, aux channel differential signals and HPD signals can be left as No Connects.



No Internal Graphics Connection Recommendation

Signal Name	Recommended Connection
CRT_RED, CRT_GREEN, CRT_BLUE	NC or GND
CRT_IRTN	GND
CRT_HSYNC, CRT_VSYNC	NC
DAC_IREF	GND through 1K ohm $\pm 5\%$ or 1%
DDC_CLK, DDC_DATA	NC

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6.1.4.2 FDI Disable Guidelines

All the FDI signals FDI_TX, FDI_FSYNC, FDI_LSYNC and FDI_INT signals on the CPU and the PCH can be left as No connect for solutions not using integrated graphics solution.

FDI Signal	Recommendation
FDI_TX[7:0]	Float or No connect
FDI_TX# [7:0]	Float or No connect
FDI_FSYNC [1:0]	Float or No connect
FDI_LSYNC [1:0]	Float or No connect
FDI_INT	Float or No connect
FDI_COMPIO	Connect to Vss
FDI_ICOMPO	Connect to Vss

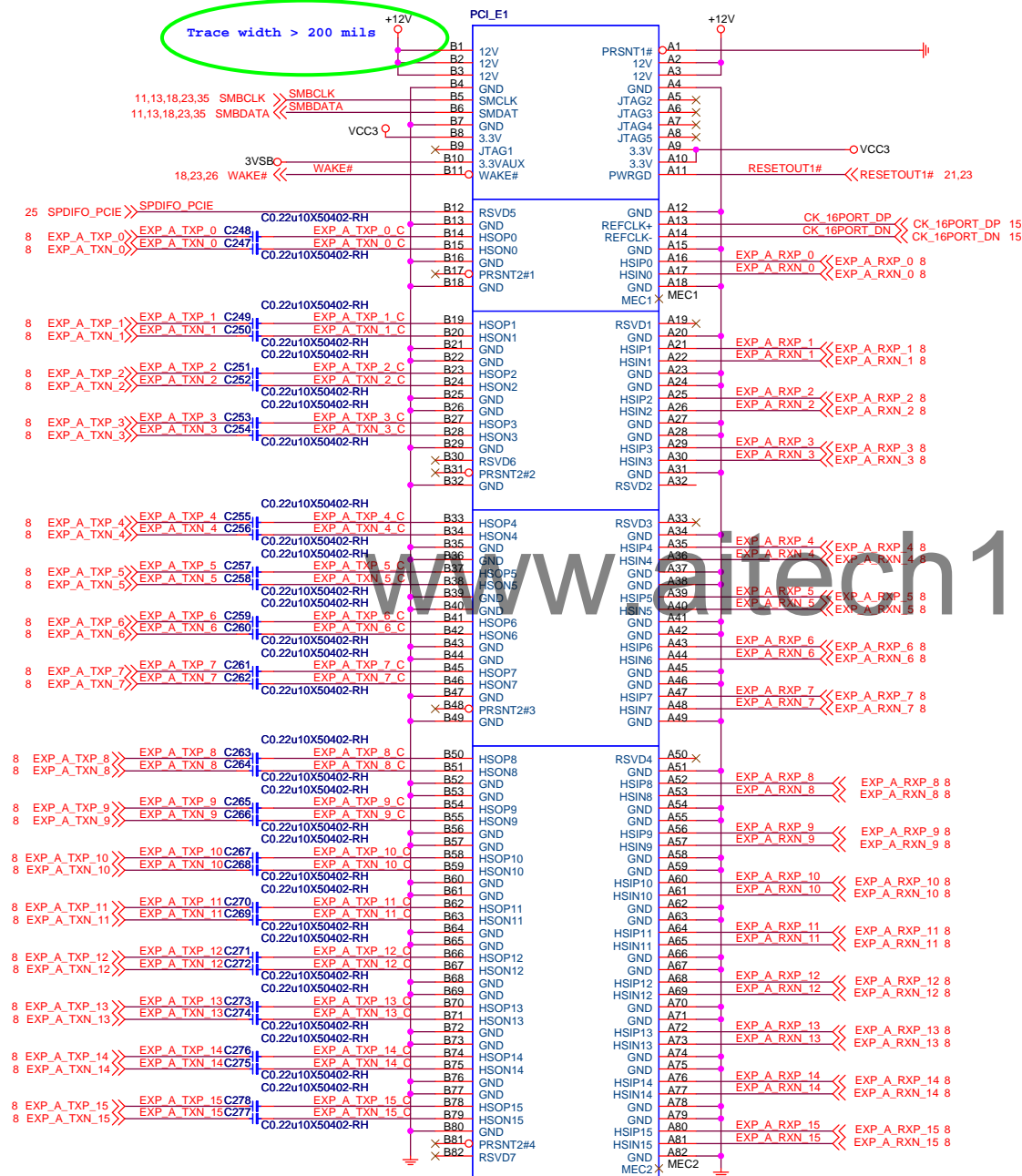


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PCI_Express X16 Slot



SLOT-PCI164P_BLACK-2PITCH-RH-16

N11-1640551-K06

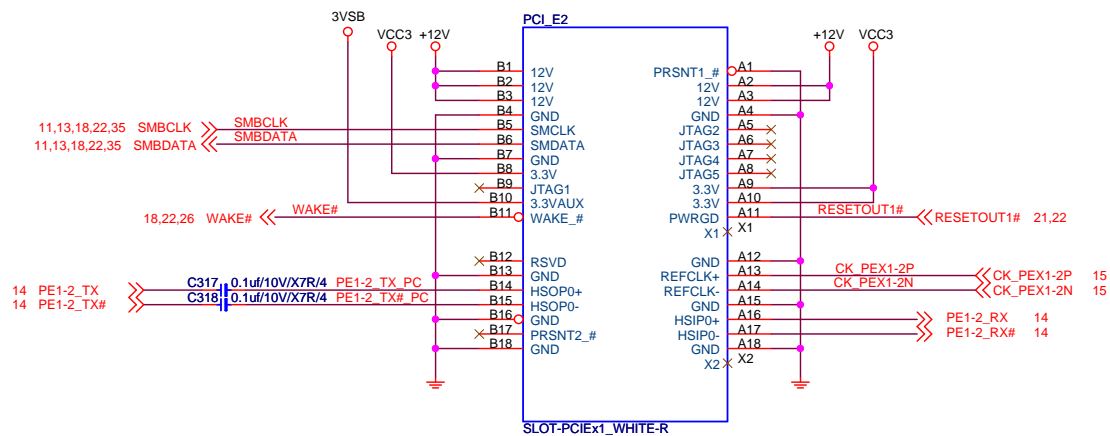


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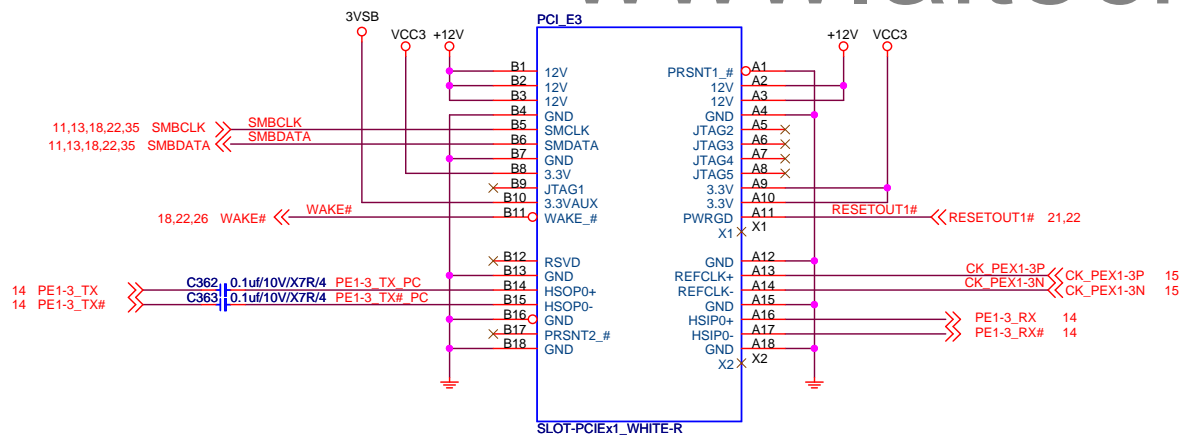
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PCI EXPRESS x1-PORT1



N11-0360091-A10

PCI EXPRESS x1-PORT2



N11-0360091-A10



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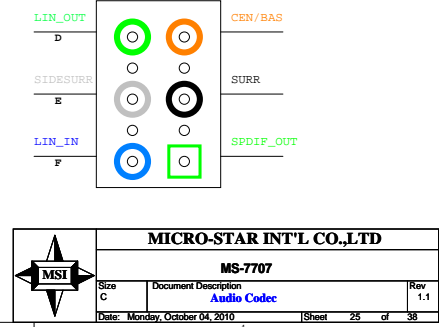
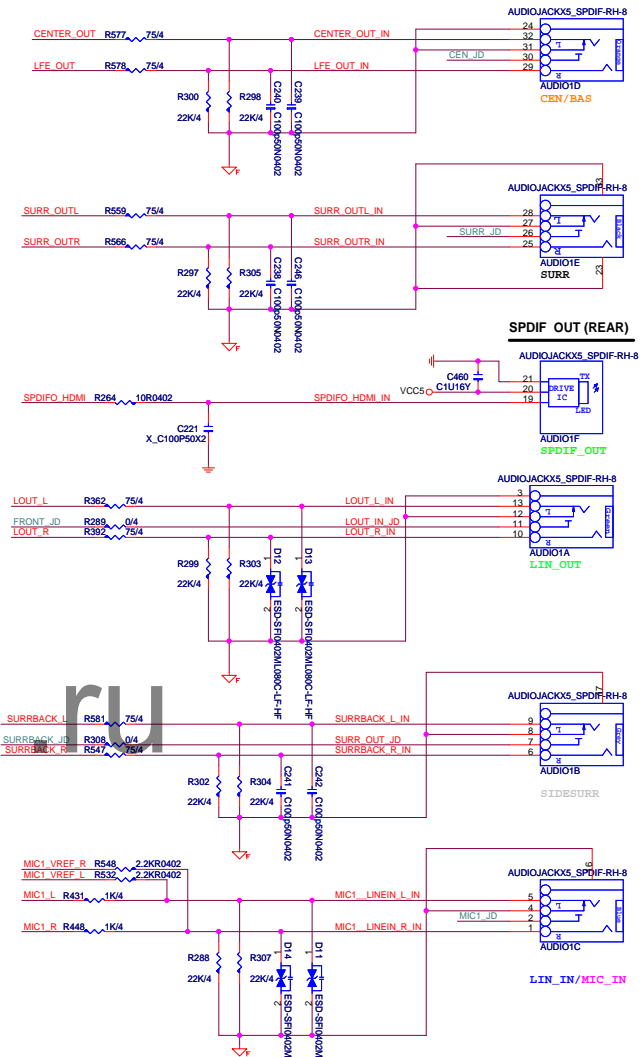
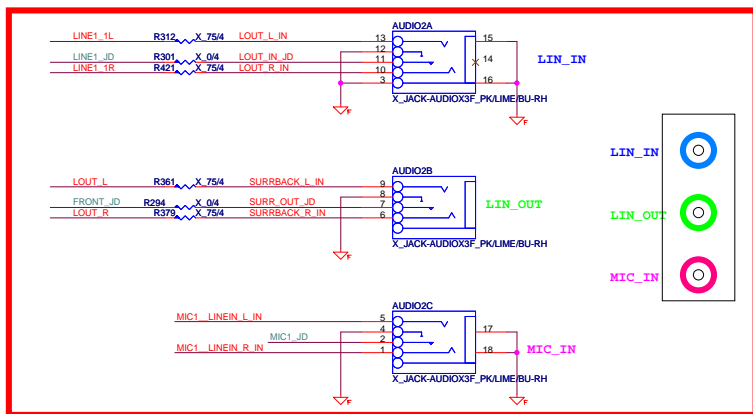
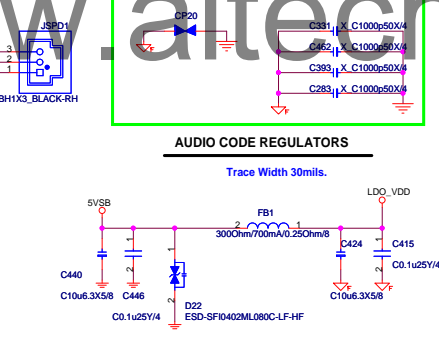
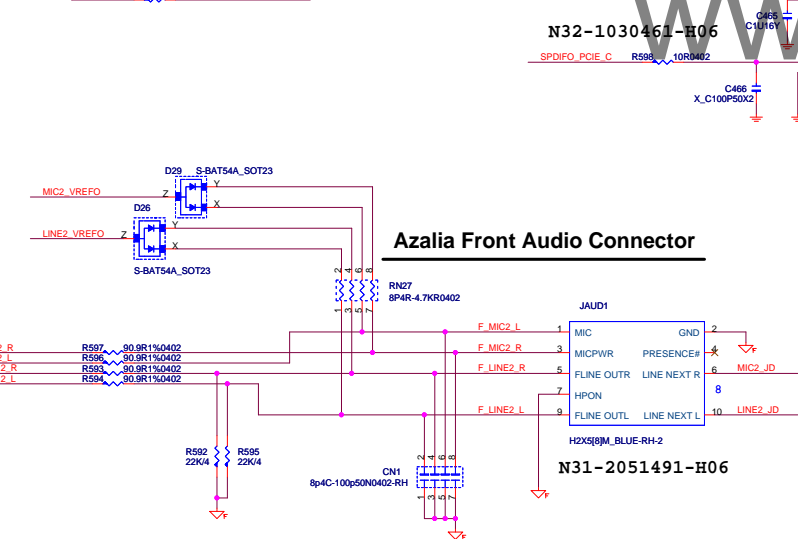
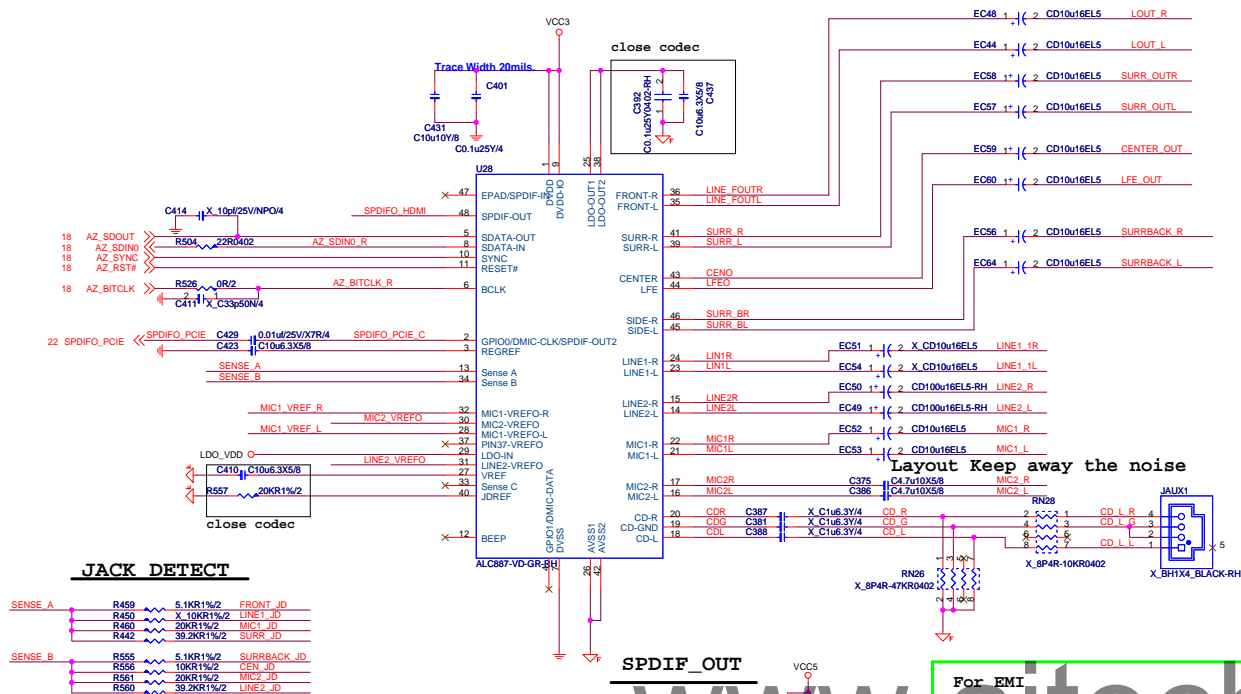
MS-7707

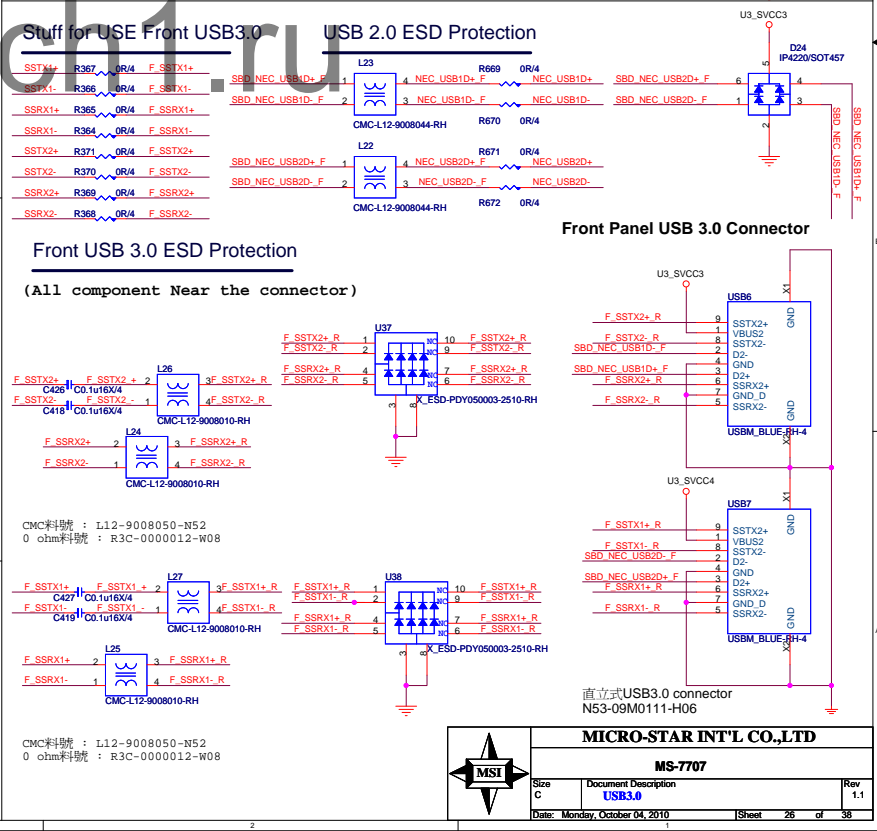
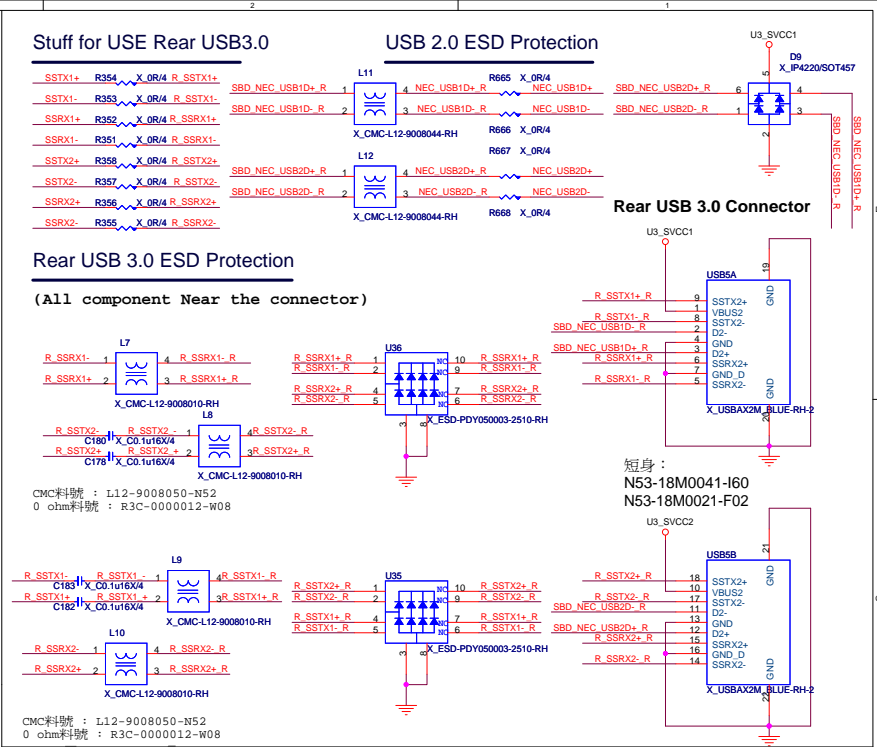
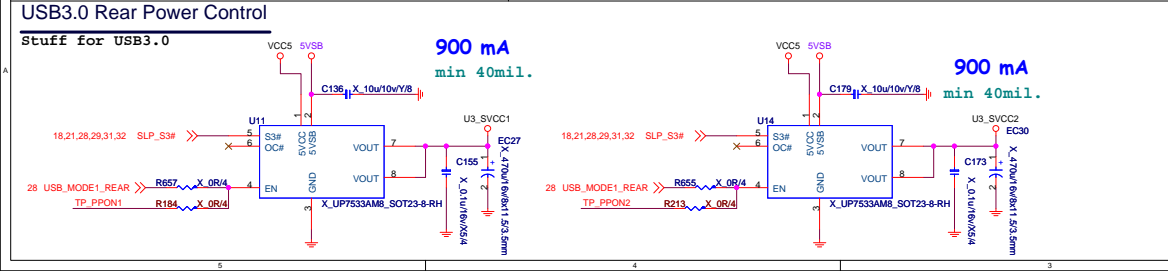
Size	Document Description	Rev
B	PCI E X1 SLOT	1.1

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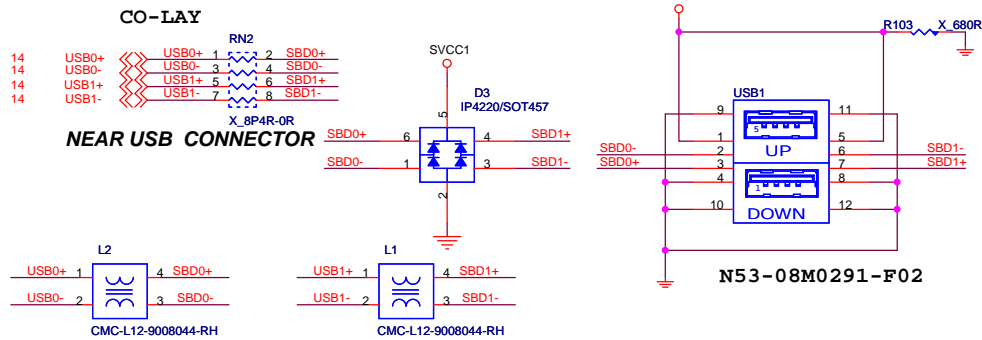
Gigabit LAN INTEL 82579

ALC887-VD-GR CODEC

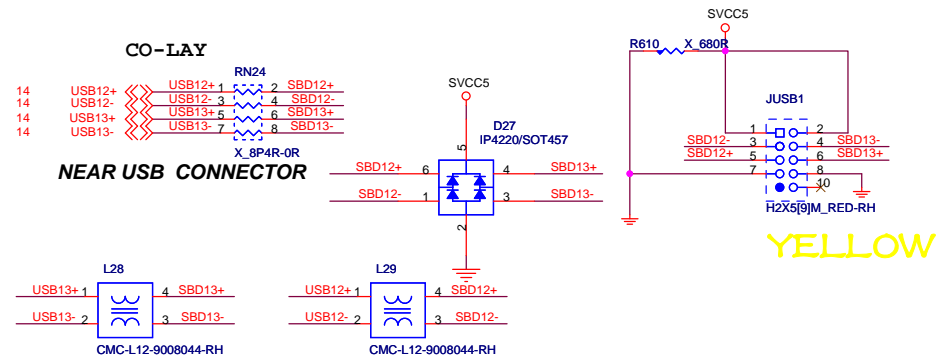




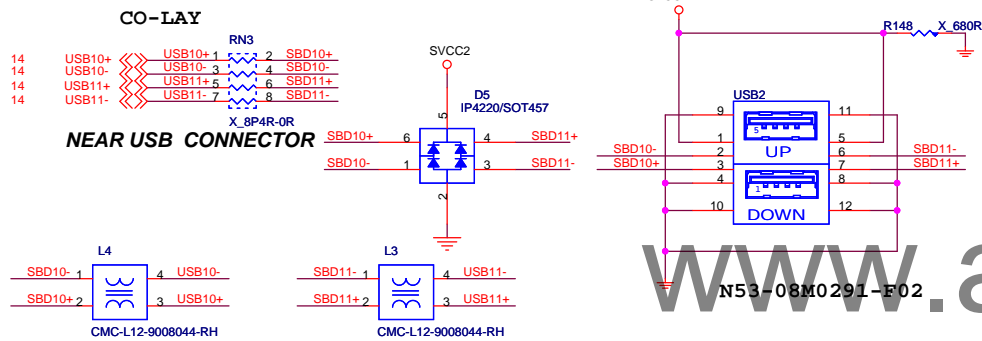
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



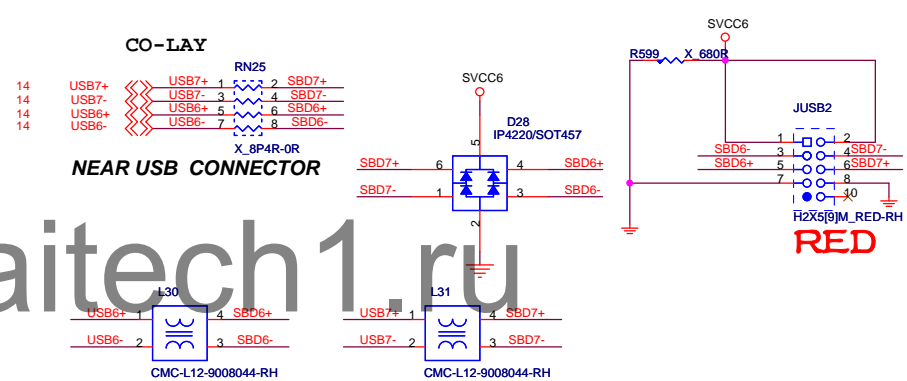
FRONT PANEL USB CONNECTOR FOR USB PORT 12,13



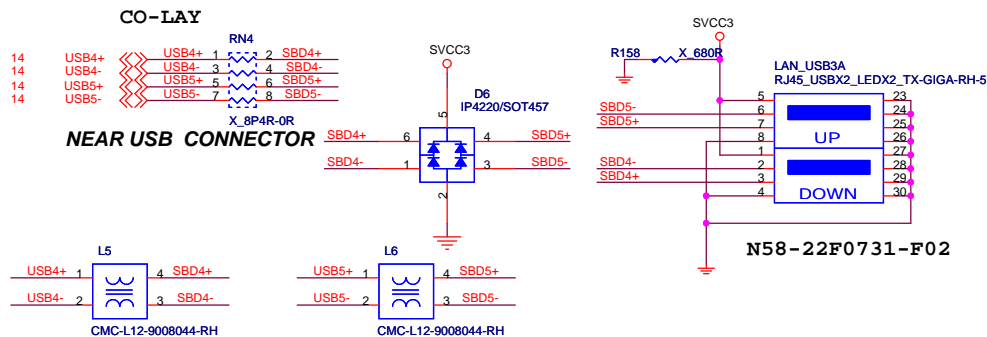
REAR PANEL USB CONNECTOR FOR USB PORT 10,11



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



REAR PANEL USB CONNECTOR FOR USB PORT 4,5



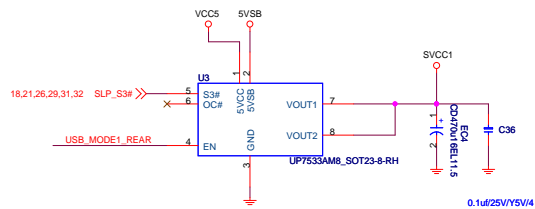
MICRO-STAR INT'L CO.,LTD

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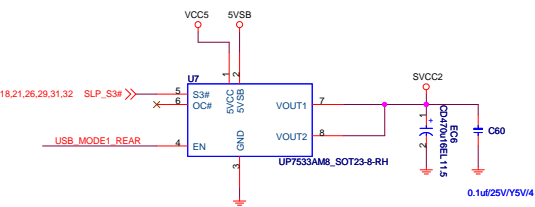
Size	Document Description	Rev
Custom	USB Conn.	1.1
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REAR POWER CONTROL

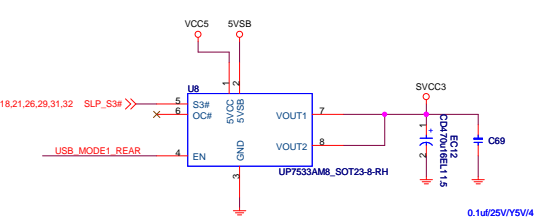
Power Circuit For USB Port 0, 1 (Connector USB1) And KB/MS



Power Circuit For USB Port 10, 11 (Connector USB2)

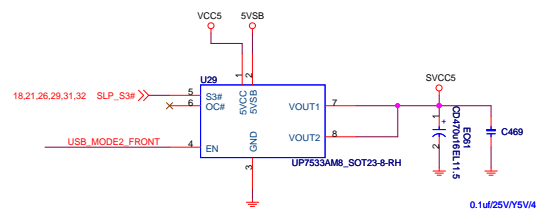


Power Circuit For USB Port 4, 5 (Connector LAN_USB3)

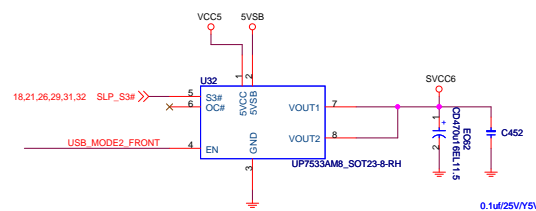


FRONT POWER CONTROL

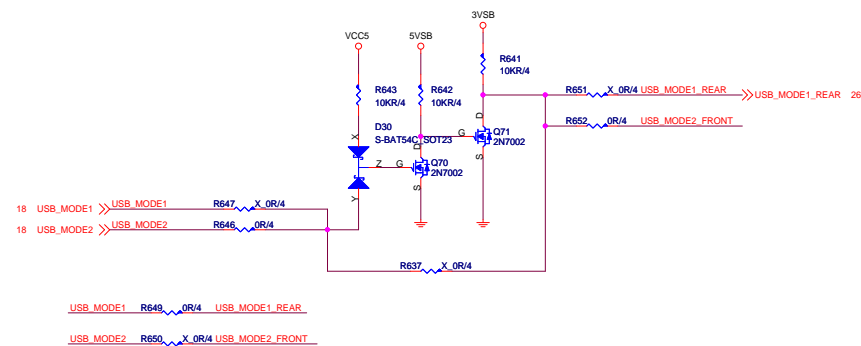
Power Circuit For USB Port 12, 13 (Pin Header JUSB1)



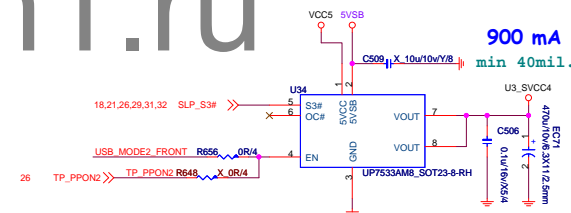
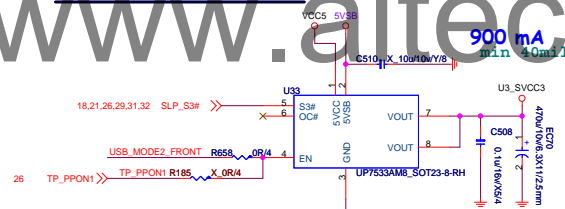
Power Circuit For USB Port 6, 7 (Pin Header JUSB2)



USB3.0 Power Control



USB3.0 Front Power Control



USB3.0 與 2.0 上件差異處

上件Front USB 3.0 時

Cfg-7707-10-USBF(線路看到的狀況)

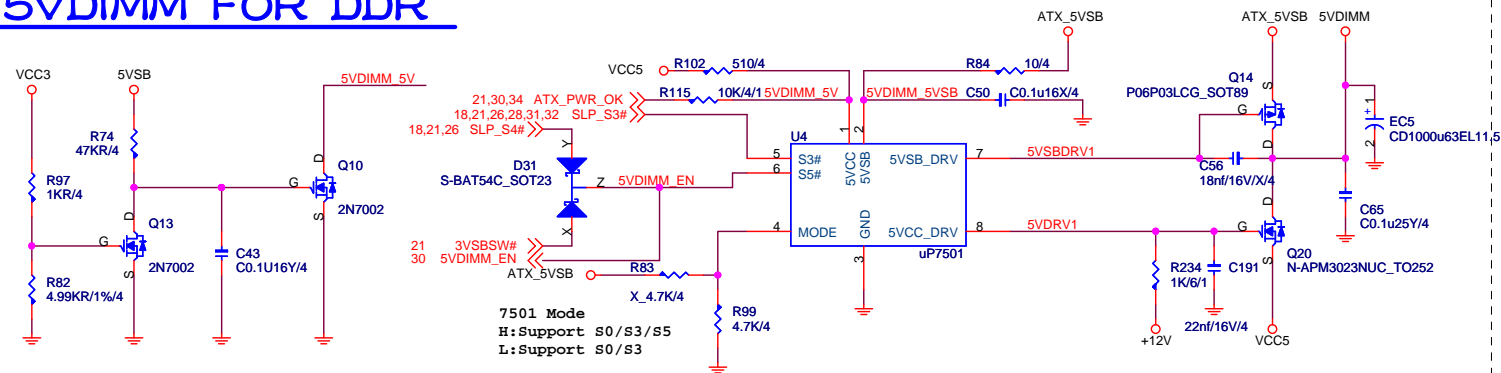
上件 Front USB3.0 與USB2.0 (Connector USB2)

上件Rear USB 3.0 時

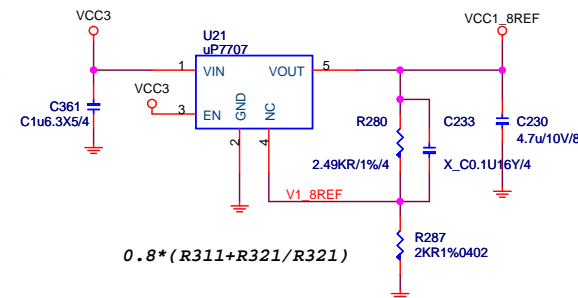
Cfg-7707-10-USBR(Rear usb 3.0 BOM 參考元件中cfg)

上件 Rear USB3.0 , 不上件USB2.0 (Connector USB2)

5VDIMM FOR DDR

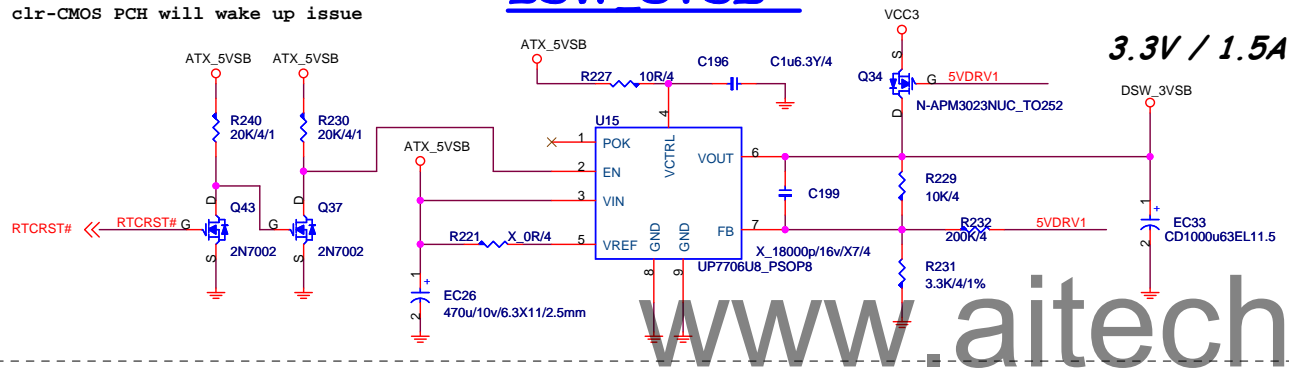


VCC1_8REF

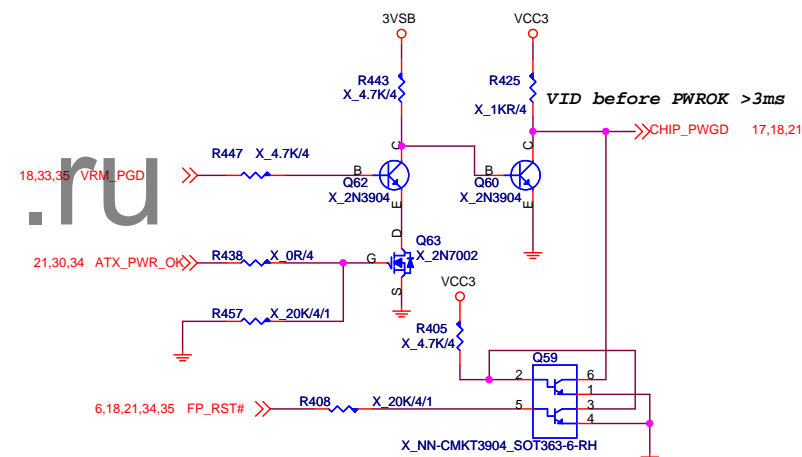


RTCRST patch circuit for
clr-CMOS PCH will wake up issue

DSW 3VSB

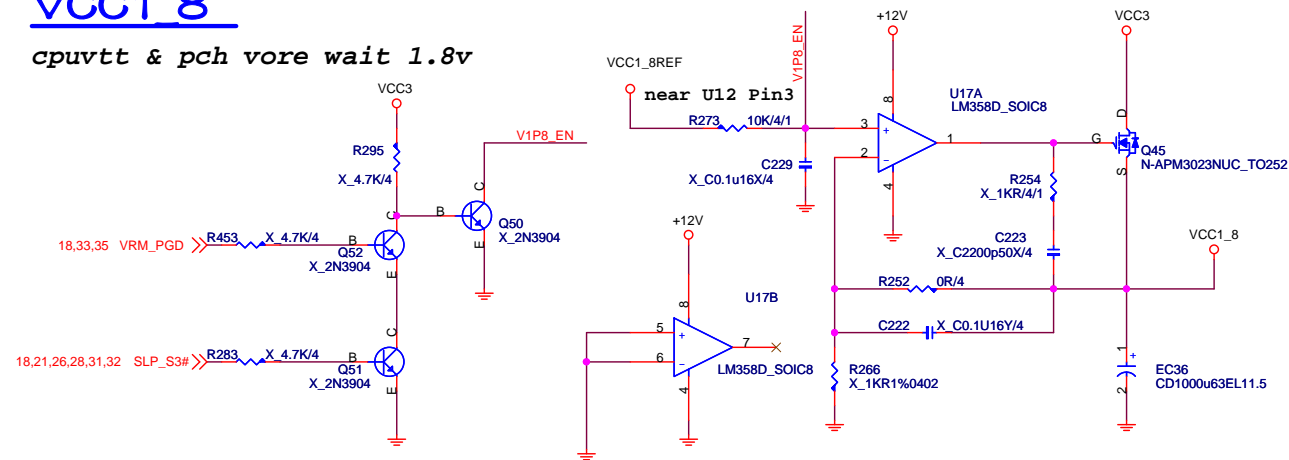


PWROK DELAY



VCC1_8

cpuvt & pch vore wait 1.8v



Update from SLP_S3# to VRM_PGD



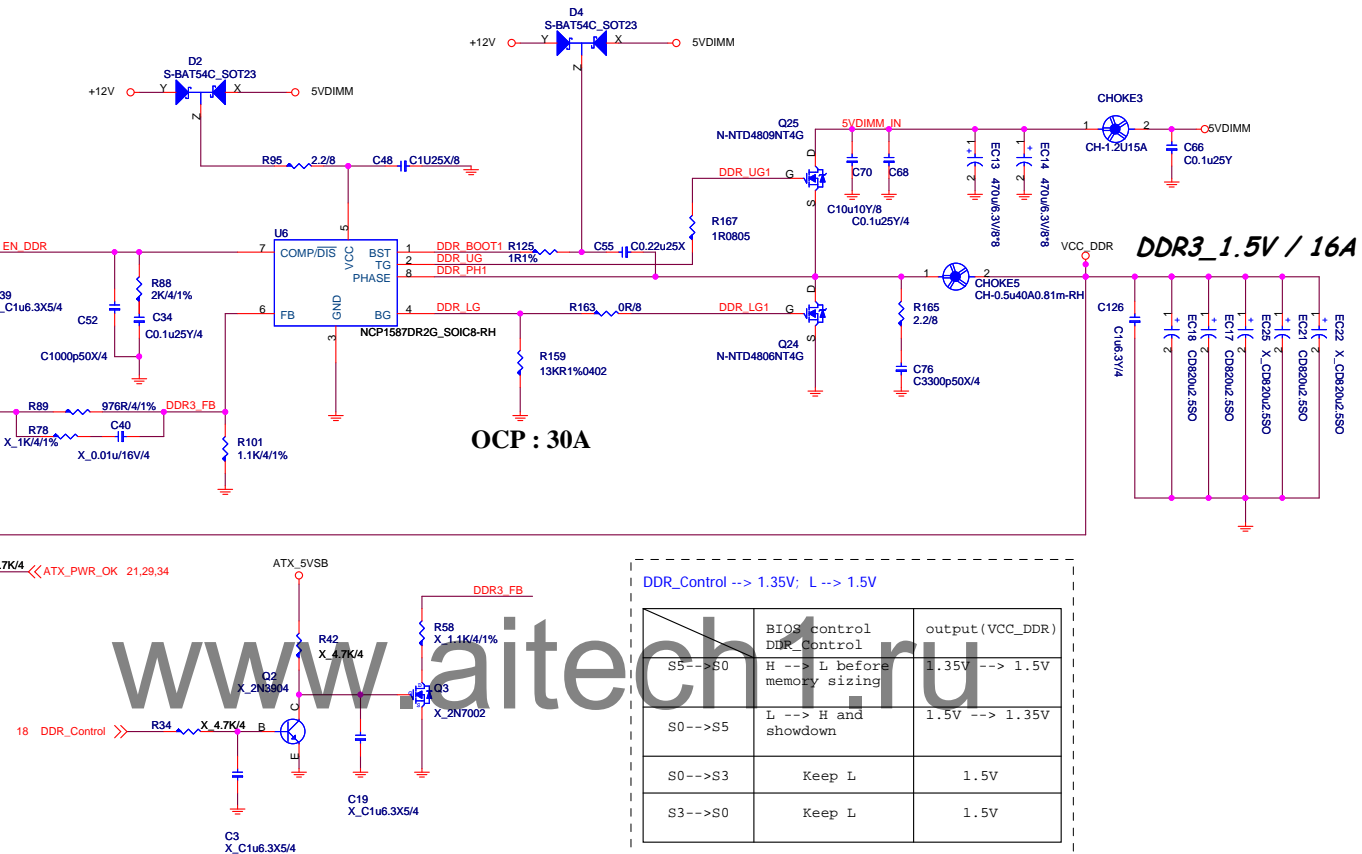
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B	ACPI Controller 1	1.1

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VTT_DDR



DDR_Control --> 1.35V; L --> 1.5V		
S5-->S0	BIOS control DDR_Control H --> L before memory sizing	output(VCC_DDR 1.35V --> 1.5V
S0-->S5	L --> H and showdown	1.5V --> 1.35V
S0-->S3	Keep L	1.5V
S3-->S0	Keep L	1.5V



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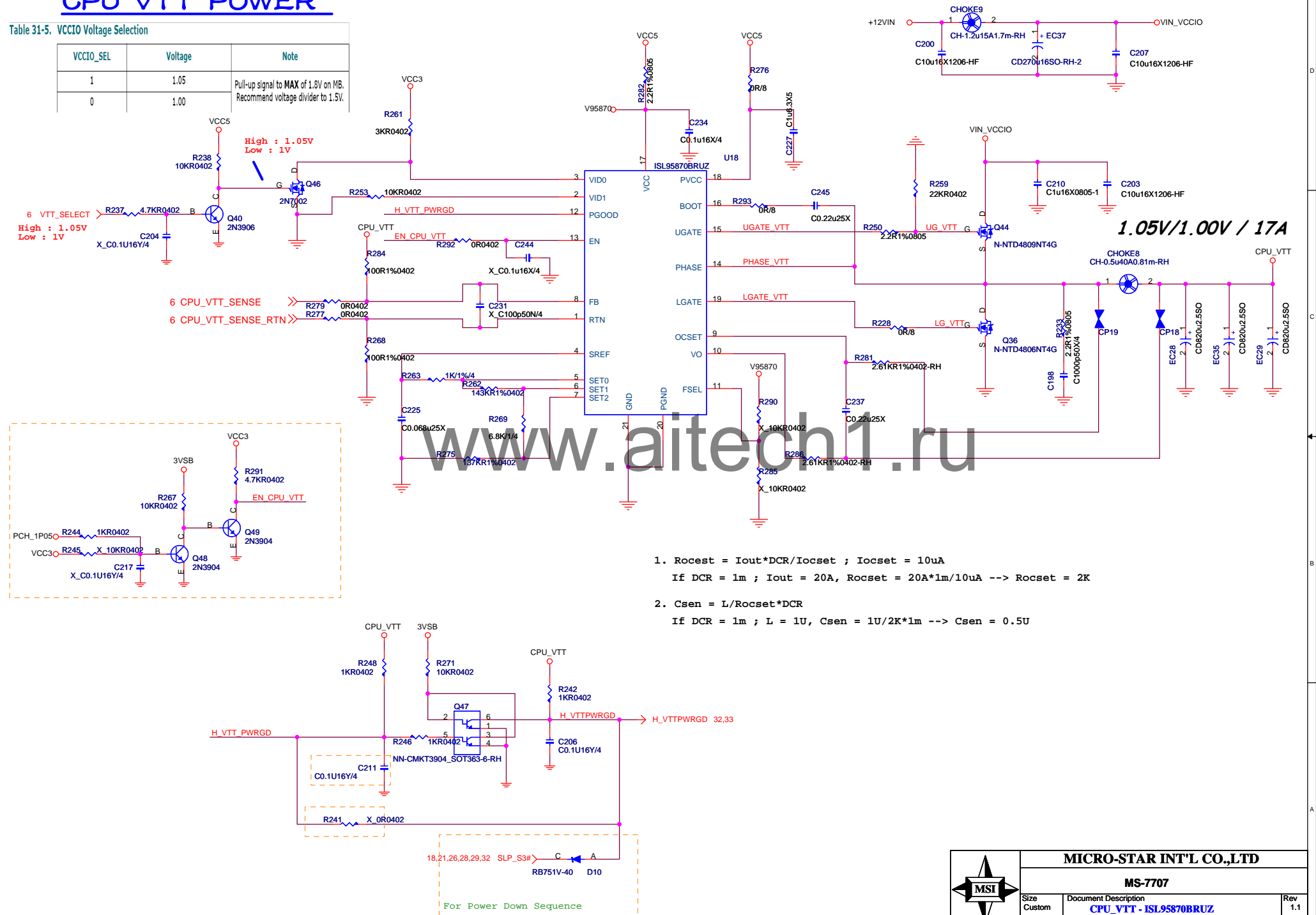
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Size Custom	Document Description DDR POWER - NCP1587	Rev 1.1
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CPU VTT POWER

Table 31-5. VCCIO Voltage Selection

VCCIO_SEL	Voltage	Note
1	1.05	Pull-up signal to MAX of 1.6V on MB. Recommend voltage divider to 1.5V.
0	1.00	



```

1. Rocset = Iout*DCR/Iocset ; Iocset = 10uA
   If DCR = 1m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K

2. Csen = L/Rocset*DCR
   If DCR = 1m ; L = 1u, Csen = 1u/2K*1m --> Csen = 0.5u

```

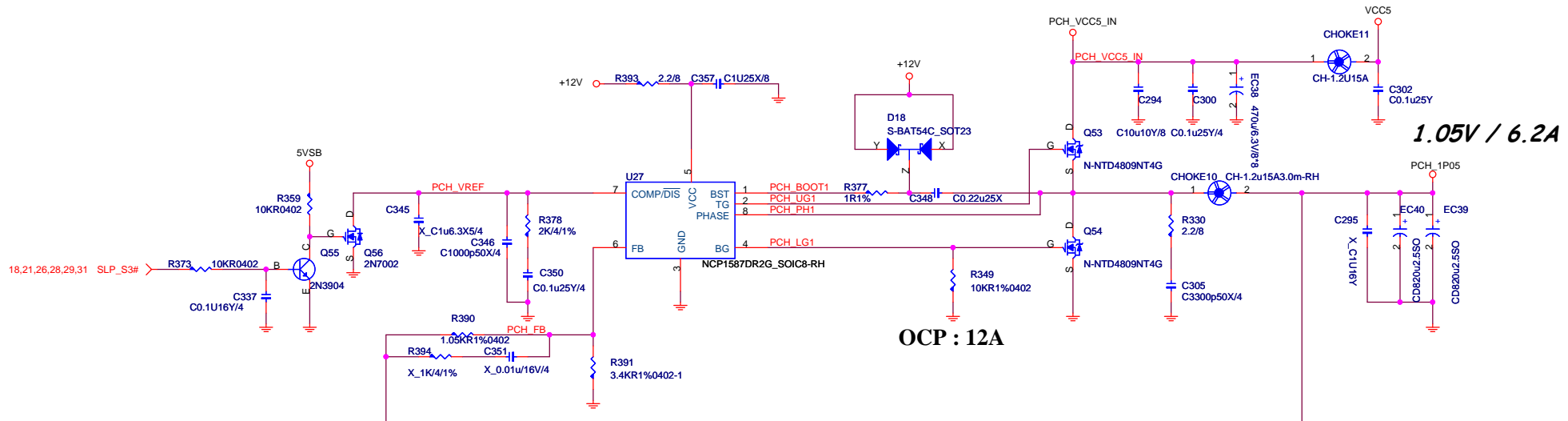


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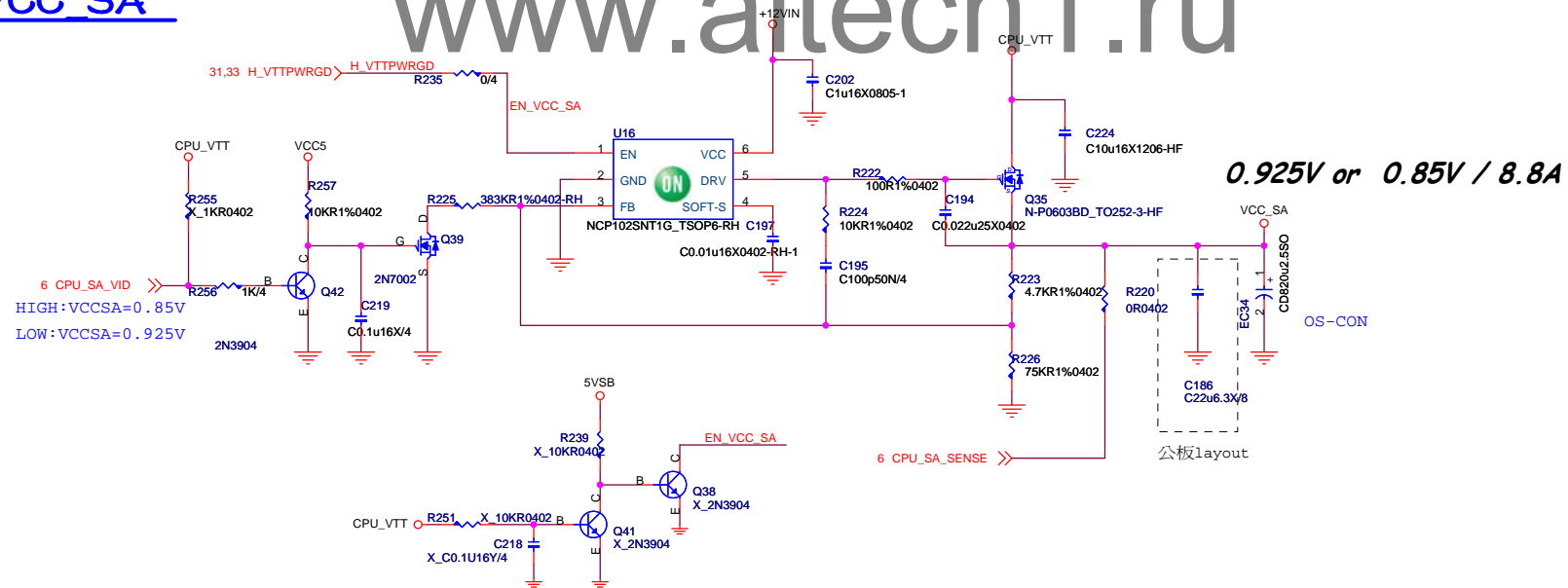
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PCH_1P05



VCC_SA



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Custom	PCH Power-NCP1587D/NCP102SNT	1.1
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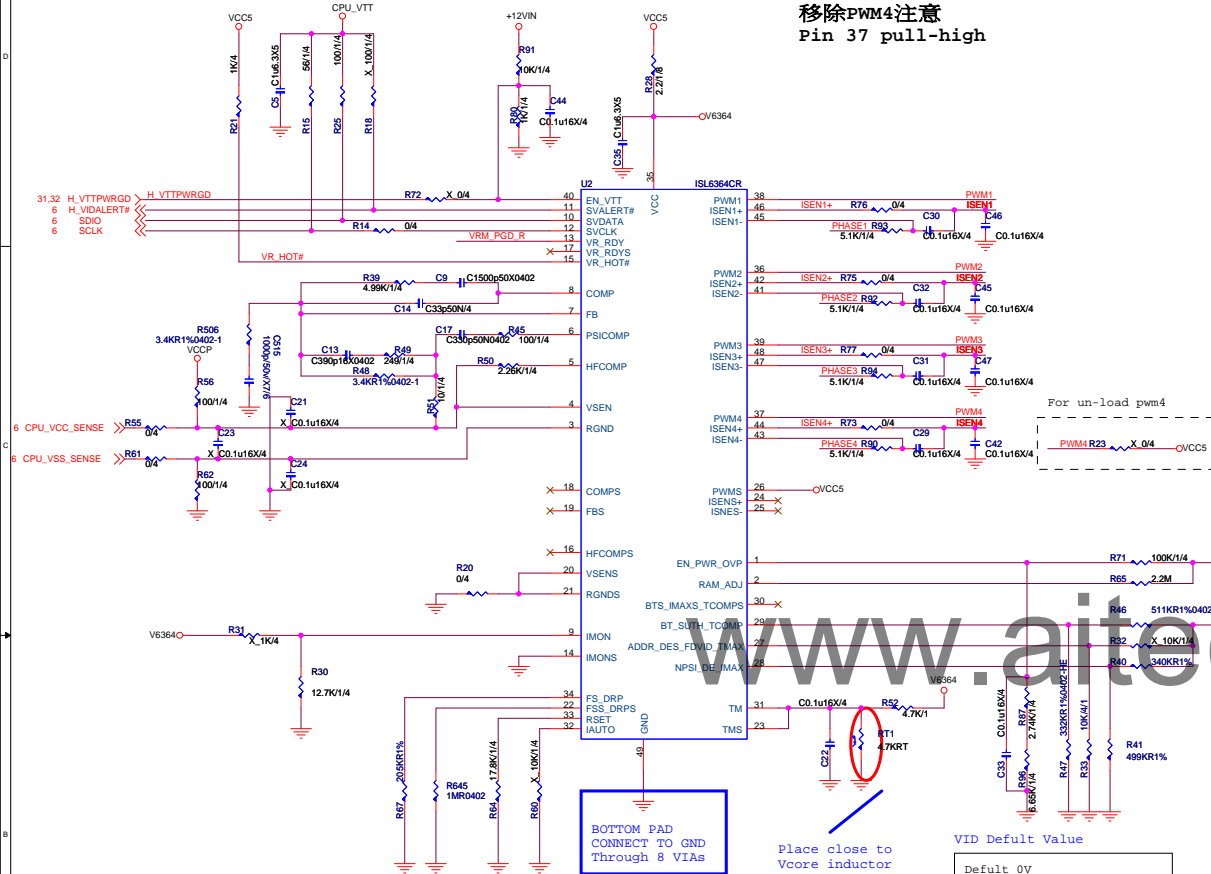
Voltage Regular Module (VRD12)

移除GPU Power pin腳注意

24,25,26,17,18,19,16,20,21,14,22,23,30

移除PWM4注意

Pin 37 pull-high



BOTTOM PAD
CONNECT TO GND
Through 8 VIAs

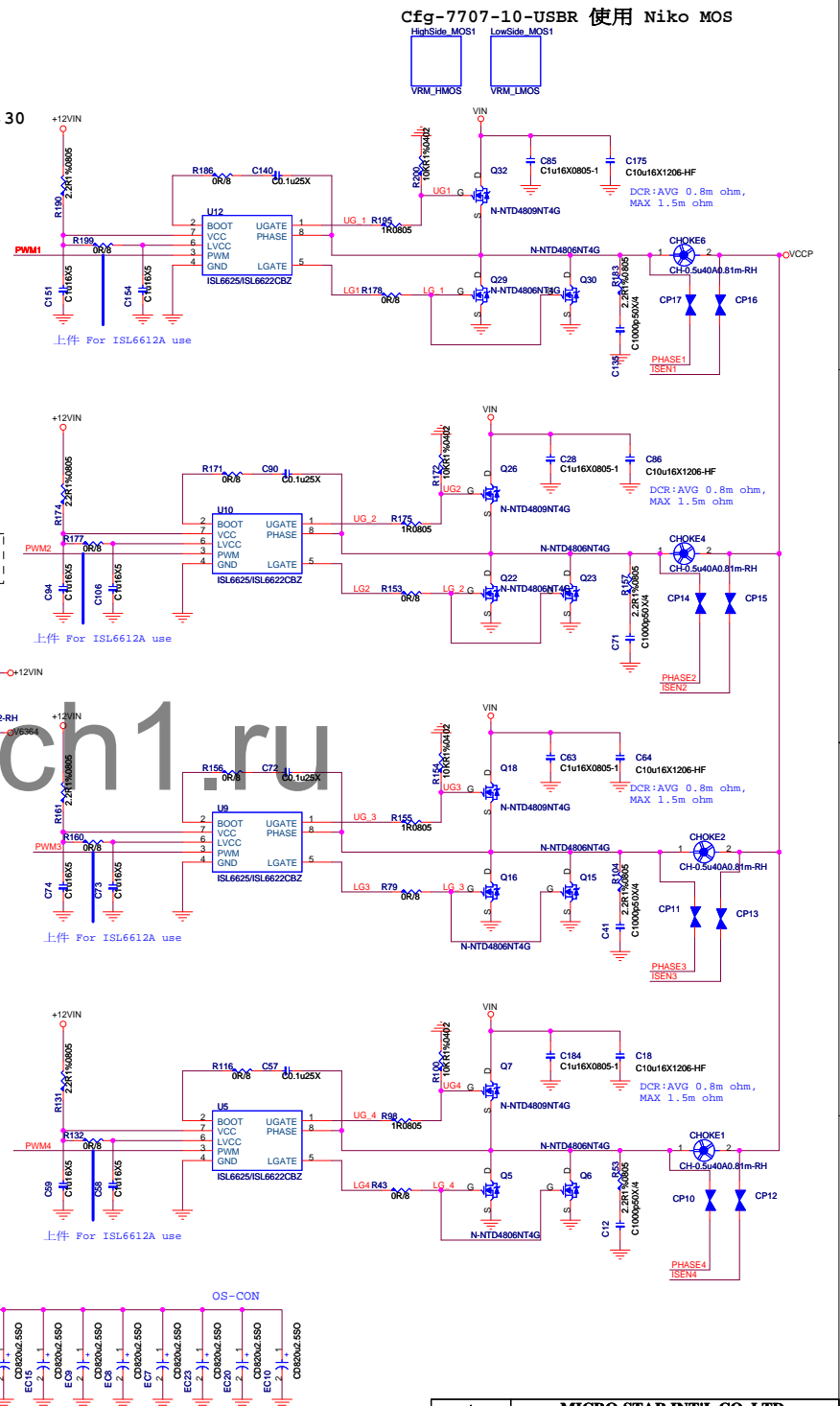
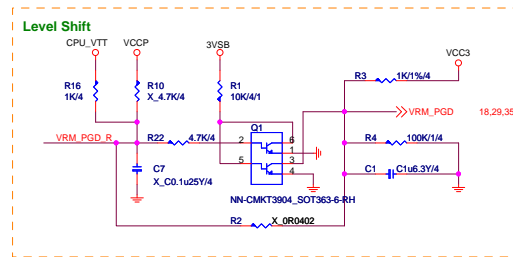
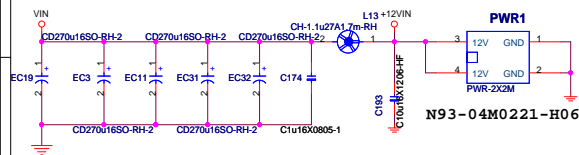
Place close to
Vcore inductor

VID Default Value

Default 0V

R46 : R11-5113T12-W08 511R

R47 : R11-3323T12-W08 332R

[illegible]

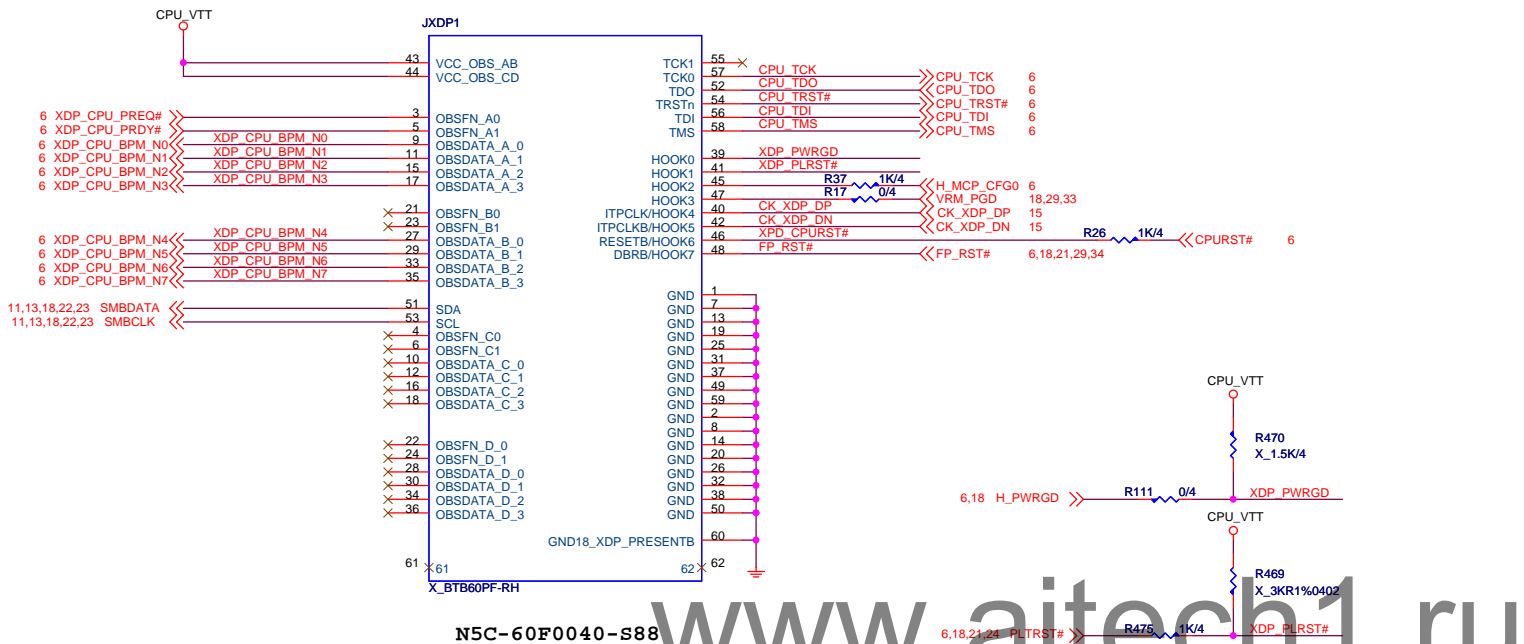
MICRO-STAR INT'L CO.,LTD

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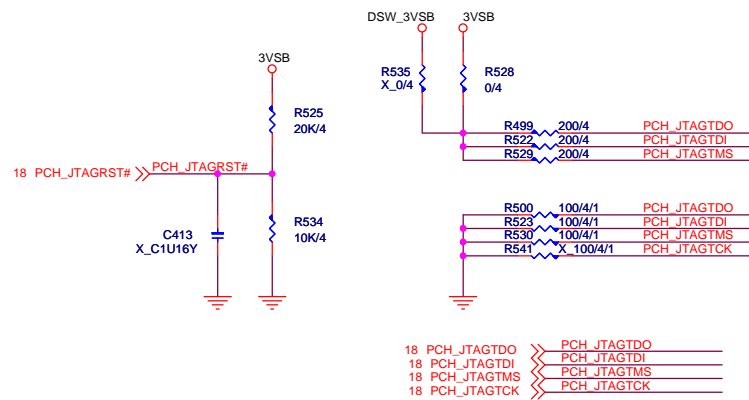
Size C	Document Description VRD12 - ISL6364 4-Phase	Rev 1.1
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CPU XDP



PCH XDP PWRGD/RESET



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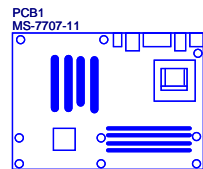
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Size Custom	Document Description CPU/PCH XDP
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Rev	1.1
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PCB



Main : P30-0770711-G37
Av1 : P30-0770711-E55

BAT1_X1



BAT-BCR2032P-RH

RUBBER_X1



X_RUBBER

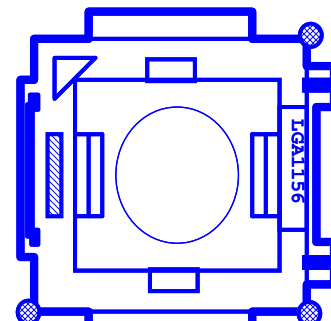
RUBBER_X2



X_RUBBER

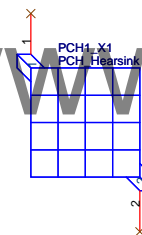
CPU SOCKET

CPU1_X1
CPU SOCKET



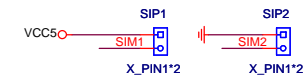
E21-7557010-F02

NB Heat-sink



E31-0401634-K08

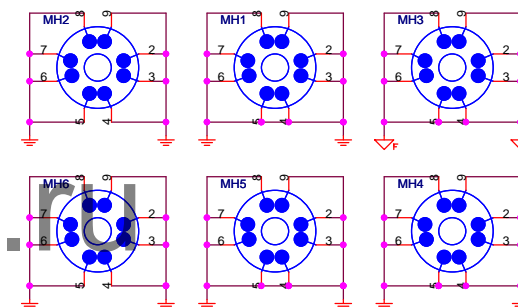
Simulation



Optical Fiducial Marks-120



Mounting Holes



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Manual & Option parts

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ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

CPU PW
12V +/-5%

VRD12 +CPU_VCCP PWM REGULATOR
--

+CPU_GFX PWM REGULATOR

+CPU_VTT PWM REGULATOR

+CPU_VCCSA PWM REGULATOR

5V_DIMM Linear REGULATOR

VCC_DDR PWM REGULATOR

PCH_1P05 PWM REGULATOR

5V_USB Linear REGULATOR

3VSB Linear REGULATOR

X1 PCIe per
+3.3V 3.0A
+12V 0.5A
+3.3Vaux 0.4A

X16 PCIe
+3.3V 3.0A
+12V 5.5A
+3.3Vaux 0.4A

USB3.0 X2 FR
VDD
5V_USB
2.0A

USB3.0 X2 RL
VDD
5V_USB
2.0A

USB X6 FR
VDD
5V_USB
3.0A

USB X6 RL
VDD
5V_USB
3.0A

SANDY BRIDGE (95W)
VCCP (CPU core series VID) 112A
VAXG (GFX core) 35A
VTT (CPU Uncore, I/O) 8.5A
VCCSA (CPU Uncore, I/O) 8.8A
VDDQ (DDR I/O) 4.5A
VccPLL (SFR supplies) 1A

Cougar Point PCH (5.5W)
V_CPU_CORE 1.05V 6.2A
VccPLL 1.05V 0.5A
Vcc3_3 3.3V 0.203A
V5REF 5V <1mA
V5REF_Sus 5V <1mA
Vcc3_3SB 3.3V 0.123A
VccADAC 3.3V 60mA
VccRTC 3.3V <1mA

HD Audio 92HD89E
+5VR 51 mA
VCC3 40 mA


LAN RTL8111E
VDD3 58mA
VDD1P2 289mA

VBAT



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